

# Compal LA-L051P

## GH52T MB Schematic Document

Rev : 1.0

2020.12.17

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2019/09/20	Deciphered Date	2020/12/31	Title	
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- Size : 2M  
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Processor**

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- Channel B  
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- PS8713

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- GEN1  
- USB3.1 Port 3  
- USB2.0 Port 3

**USB3 Re-driver**  
- PS8713

**USB3.1 - JUSB 2**  
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**USB3 Re-driver**  
- PS8713

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Vcc Ra	3.3V +/- 5% 100K +/- 1%	EC Board ID Table for AD channel				
Board ID	Rb	Vmin	Vtyp	Vmax	EC AD	
0	0		0.000 V	0.300 V	0x00 - 0x13	
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x14 - 0x1E	SD034120280
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25	SD034150280
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30	SD034200280
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A	SD034270280
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45	SD034330280
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54	SD034430280
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64	SD034560280
8	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 - 0x76	SD034750280
9	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77 - 0x87	SD034100380
10	130K +/- 1%	1.849 V	1.865 V	1.881 V	0x88 - 0x96	SD034130380
11	160K +/- 1%	2.015 V	2.031 V	2.046 V	0x97 - 0xA4	SD034160380
12	200K +/- 1%	2.185 V	2.200 V	2.215 V	0xA5 - 0xAF	SD034200380
13	240K +/- 1%	2.316 V	2.329 V	2.343 V	0xB0 - 0xB7	SD000001B80
14	270K +/- 1%	2.395 V	2.408 V	2.421 V	0xB8 - 0xBF	SD000000G280
15	330K +/- 1%	2.521 V	2.533 V	2.544 V	0xC0 - 0xC9	SD034330380
16	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA - 0xD4	SD000000WM80
17	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD5 - 0xDD	SD034560380
18	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDE - 0xF0	SD000000AL80
19	NC	3.000 V	3.000 V		0xFF1 - 0xFF	

	*PCB Version *Key board type
Board ID	PCB Revision
0	Rev0.1_H35
1	Rev0.1_UP3
2	
3	
4	Rev1.0_H35
5	Rev1.0_UP3
6	
8	Rev0.1_H35+RGB
9	Rev0.1_UP3+RGB
10	
11	
12	Rev1.0_H35+RGB
13	Rev1.0_UP3+RGB
14	
15	
16	
17	
18	
19	

STATE	SIGNAL	SLP_S0#	CPU_C10_GATE#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)		HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		HIGH	HIGH	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		HIGH	HIGH	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft t OFF)		HIGH	HIGH	LOW	LOW	LOW	ON	OFF	OFF	OFF
SOIX		LOW	LOW	HIGH	HIGH	HIGH	ON	ON	ON	ON

Power Plane	Descript i on	S0	S0ix	S3	S4/S5
+19V_ADPIN_P1	Adapter power supply	N/A	N/A	N/A	N/A
+20V_PDVIN	PD USB-C power supply	N/A	N/A	N/A	N/A
+12.6V_BATT	Bat tery power supply	N/A	N/A	N/A	N/A
+19VB	AC or bat tery power rail for power circuit	N/A	N/A	N/A	N/A
+VCCIN	Core voltage for CPU	ON	OFF	OFF	OFF
+VCCIN_AUX	CPU and PCH merged auxiliary power rail	ON	OFF	OFF	OFF
+0.6V_VDDQ	LPDDR4x +0.6V power rail(VDDQ)	ON	OFF	OFF	OFF
+1.05V_VCCST	Sustain voltage for CPU standby modes	ON	ON	ON	OFF
+1.05VS_VCCSTG	Gated sustain voltage for CPU standby modes	ON	OFF	OFF	OFF
+1.2V_VCCPLL_OC	+1.2V power rail for CPU digital PLL	ON	OFF	ON	OFF
+1.35VS_VRAM	+1.35VS power rail for GPU	ON	OFF	OFF	OFF
+1.1V_VDDQ	LPDDR4x +1.1V power rail (VDD2)	ON	ON	ON	OFF
+1.8V	LPDDR4x +1.8V power rail(VDD1)	ON	ON	ON	OFF
+1.8V_PRIM_SOC	TCSS/AGSH TypeC sub system / CPU analog power supply	ON	OFF	OFF	OFF
+1.8VALW	System +1.8V power rail	ON	ON	ON	ON*
+1.8VS	System +1.8VS power rail	ON	ON	OFF	OFF
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON*
+3V_PRIM	+3VALW power for PCH suspend rails	ON	ON	ON	ON*
+3VS	System +3VS power rail	ON	ON	OFF	OFF
+1.8VS_DGPU_AON	+1.8VS power rail for GPU(AON rails)	ON	OFF	OFF	OFF
+1.8VS_DGPU	+1.8VS power rail for GPU	ON	OFF	OFF	OFF
+VGA_CORE	Power rail for GPU	ON	OFF	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON	ON*
+5VS	System +5VS power rail	ON	ON	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF

BUS	Device	Address(7 bit)	Address(8bit)	
			Write	Read
SOC_CK/DA (Port0)				
SOC_CK/DA (Port3)	TM-P3393-003 (Touch Pad)			
SOC_SMBCLK	DIMM1	0xA0	0xA1	0xA0
	DIMM2	0xA3	0xA4	0xA3
EC_CK/DA (Port0) (+3VLP)	BQ24780 (Charger IC)	0x12		
	BATTERY PACK	0x16		
EC_CK/DA (Port1) (+3VS)	TGL-U / PCH LP	TBD		
SOC_SML1CK/DA (+3VALW)	N18P-G61-A/GN20P (VGA)	0x9E		
	Thermal Sensor (NCT7718W)	0x98	1001_1001b	1001_1000b
	Thermal Sensor (G781)	0x9A	1001_1011b	1001_1010b
EC_CK/DA (Port2)	LED Driver (59116F)	0xC0		
EC_CK/DA (Port3)	TI PD	0x42	0100_0011b	0100_0010b
EC_CK/DA (Port4)	N/A (Set GPIO)			

V : Must V : Options

Item (X43 / X76)	BOM Structure	Item (X43 / X76)	BOM Structure
Unpop	@	eDP-TS USB	USBTS@
Connector	CONN@	eDP-TS I2C	I2CTS@ V
PCB	DA@ V	mDP	DP@
TGL-UP3(GH52T)		Intel CNVi	CNVi@ V
FH8069004530104 SRK02	I71165MP@ V	FOR UART debug	UART@
FH8069004531301 SRK05	I51135MP@ V	FOR EVT EC debug	DEBUG@ V
TGL-H35(GH51H/GH71H)		Finger Print	FP@
FH8069004600005 QWL2	I511300HQs@ V	KB LED driver	LED14P@ V
FH8069004599910 QWKW	I711370HQs@ V	Thermal sensor	TMS@ V
FH8069004599909 QWKV	I711375HQs@ V	GLITCH	GLITCH@ V
FH8069004600005 SRKH6	I511300HMP@ V	CMC	CMC@ V
FH8069004599910 SRKH5	I711370HMP@ V	Power PRIM Design	PREM@ V
N18P GPU		TypeC Port	TypeC@ V
N18P-G61-A-A1 PS GPU	N18PAQS@	HDD	HDD@ V
N18P-G61-A-A1 GPU	N18PAMP@ V		
dGPU circuit	VGA@ V	GH51H Bracket	GH51H@ V
N18PG-61-A GPU&Part	N18PA@ V	GH52T Bracket	GH52T@ V
GN20 Part	N20P@		
GN20P0 GPU	N20P0@		
GN20P1 GPU	N20P1@		
GPU OVRM	OVRM@ V	EC Board ID	
SPI 1 Load	1LD@ V	Rev1.0 H35 without RGB	H35WORGB@
SPI 2 Load	2LD@	Rev1.0 H35 with RGB	H35WRGB@
TPM	TPM@	Rev1.0 UP3 without RGB	UP3WORGB@
Vpro funct i on	VPRO@	Rev1.0 UP3 with RGB	UP3WRGB@

43 Level	Descript i on	BOM Structure
431AQTBOLO1	GH51H PG61A I5 300	CMC@/GLITCH@/1LD@/I2CTS@/VGA@/PREM@/X4E@/DP@/OVRM@/TypeC@/CNVi@/DEBUG@/EVT@/LED14P@/TMS@/FF@/HDD@/CHG@/N18PA@/I511300H@/X76SAM@/X76UPIGEN1@/DA@
431AQTBOLO2	GH51H PG61A I7 370	CMC@/GLITCH@/1LD@/I2CTS@/VGA@/PREM@/X4E@/DP@/OVRM@/TypeC@/CNVi@/DEBUG@/EVT@/LED14P@/TMS@/FF@/HDD@/CHG@/N18PA@/I711370H@/X76SAM@/X76UPIGEN1@/DA@
431AQTBOLO3	GH51H PG61A I7 375	CMC@/GLITCH@/1LD@/I2CTS@/VGA@/PREM@/X4E@/DP@/OVRM@/TypeC@/CNVi@/DEBUG@/EVT@/LED14P@/TMS@/FF@/HDD@/CHG@/N18PA@/I711375H@/X76SAM@/X76UPIGEN1@/DA@
431AQTBOLO4	GH51H PG61A SRKH6	CMC@/GLITCH@/1LD@/I2CTS@/VGA@/PREM@/X4E@/OVRM@/TypeC@/CNVi@/DEBUG@/TMS@/HDD@/CHG@/N18PA@/I511300HMP@/X76SAM@/X76UPIGEN1@/DA@/N18PAMP@/H35M@/RG@/GH51H@
431AQTBOLO5	GH51H PG61A SRKH5	CMC@/GLITCH@/1LD@/I2CTS@/VGA@/PREM@/X4E@/OVRM@/TypeC@/CNVi@/DEBUG@/TMS@/HDD@/CHG@/N18PA@/I511300HMP@/X76SAM@/X76UPIGEN1@/DA@/N18PAMP@/H35M@/RG@/GH51H@
431AQTBOLO6	GH51H PG61A SRKH6 R	CMC@/GLITCH@/1LD@/I2CTS@/VGA@/PREM@/X4E@/OVRM@/TypeC@/CNVi@/DEBUG@/TMS@/HDD@/CHG@/N18PA@/I511300HMP@/X76SAM@/X76UPIGEN1@/DA@/N18PAMP@/H35M@/RG@/GH51H@/LE
431AQTBOLO7	GH51H PG61A SRKH5 R	CMC@/GLITCH@/1LD@/I2CTS@/VGA@/PREM@/X4E@/OVRM@/TypeC@/CNVi@/DEBUG@/TMS@/HDD@/CHG@/N18PA@/I711370HMP@/X76SAM@/X76UPIGEN1@/DA@/N18PAMP@/H35M@/RG@/GH51H@/LE
431AQTBOLO8	GH51H PG61A I5 300 QS	CMC@/GLITCH@/1LD@/I2CTS@/VGA@/PREM@/X4E@/OVRM@/TypeC@/CNVi@/DEBUG@/TMS@/HDD@/CHG@/N18PA@/I711370HMP@/X76SAM@/X76UPIGEN1@/DA@/N18PAMP@/H35M@/RG@/GH51H@/LE
431AQTBOLO9	GH51H PG61A I7 370 QS	CMC@/GLITCH@/1LD@/I2CTS@/VGA@/PREM@/X4E@/OVRM@/TypeC@/CNVi@/DEBUG@/TMS@/HDD@/CHG@/N18PA@/I711370HMP@/X76SAM@/X76UPIGEN1@/DA@/N18PAMP@/H35M@/RG@/GH51H@/LE
431AQTBOLO10	GH51H PG61A I5 300 QS R	CMC@/GLITCH@/1LD@/I2CTS@/VGA@/PREM@/X4E@/OVRM@/TypeC@/CNVi@/DEBUG@/TMS@/HDD@/CHG@/N18PA@/I511300HMP@/X76SAM@/X76UPIGEN1@/DA@/N18PAMP@/H35M@/RG@/GH51H@/LE
431AQTBOLO11	GH51H PG61A I7 370 QS R	CMC@/GLITCH@/1LD@/I2CTS@/VGA@/PREM@/X4E@/OVRM@/TypeC@/CNVi@/DEBUG@/TMS@/HDD@/CHG@/N18PA@/I511300HMP@/X76SAM@/X76UPIGEN1@/DA@/N18PAMP@/H35M@/RG@/GH51H@/LE
431AQTBOLO51	GH52T PG61A SRK02	CMC@/GLITCH@/1LD@/I2CTS@/VGA@/PREM@/X4E@/DP@/OVRM@/TypeC@/CNVi@/DEBUG@/EVT@/LED14P@/TMS@/FF@/HDD@/CHG@/N18PA@/I711375H@/X76SAM@/X76UPIGEN1@/DA@
431AQTBOLO52	GH52T N18PG61A SRK05	CMC@/GLITCH@/1LD@/I2CTS@/VGA@/PREM@/X4E@/DP@/OVRM@/TypeC@/CNVi@/DEBUG@/EVT@/LED14P@/TMS@/FF@/HDD@/CHG@/N18PA@/I711375H@/X76SAM@/X76UPIGEN1@/DA@
431AQTBOLO53	GH52T N18PG61A SRK02	CMC@/GLITCH@/1LD@/I2CTS@/VGA@/PREM@/X4E@/DP@/OVRM@/TypeC@/CNVi@/DEBUG@/EVT@/LED14P@/TMS@/FF@/HDD@/CHG@/N18PA@/I711375H@/X76SAM@/X76UPIGEN1@/DA@

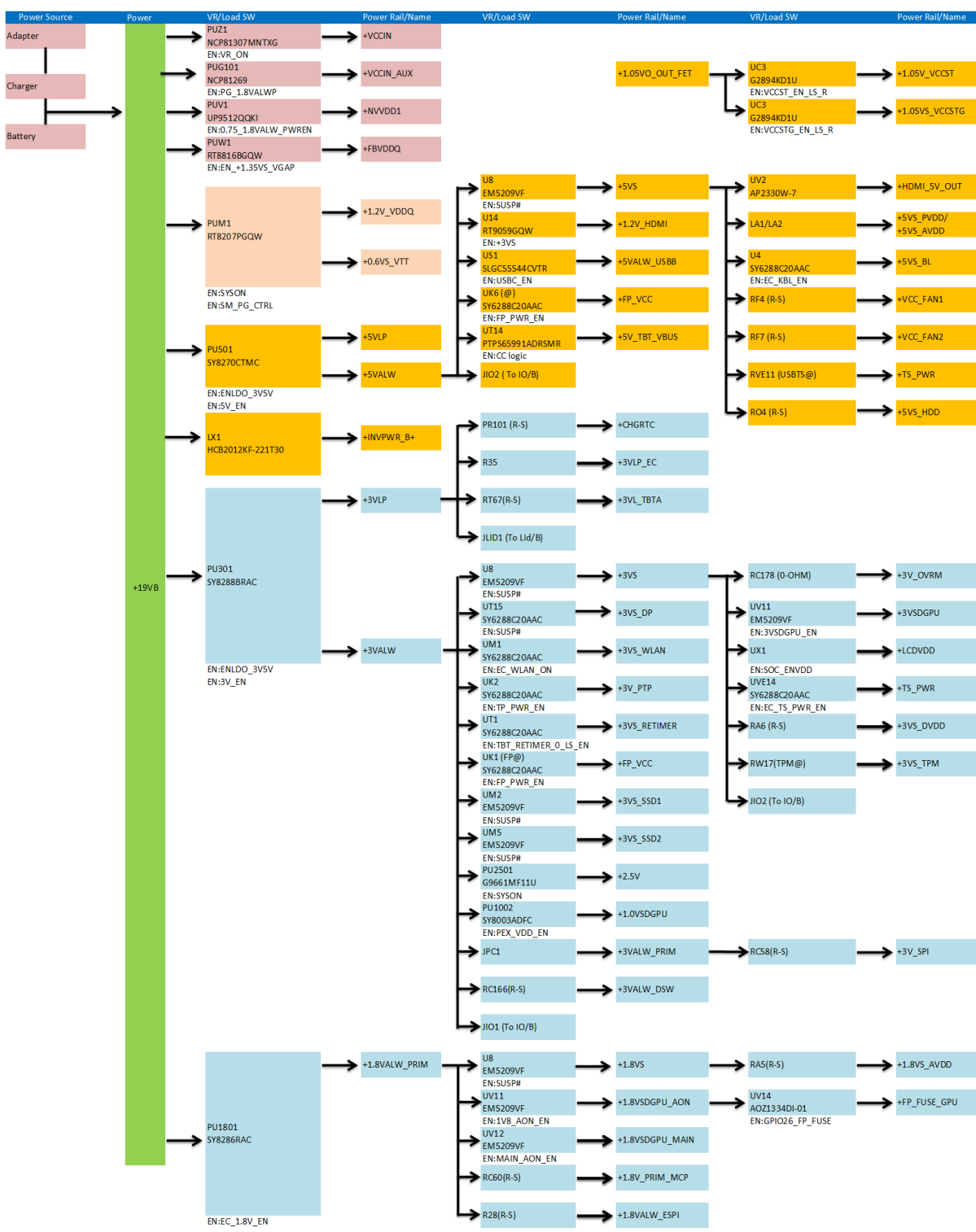
Item (X4E) pop	BOM Structure
EMI requirement	EMI@ V
EMC requirement	EMC@ V
ESD requirement	ESD@ V
RF require reserve	RF@ V
FP EMC requirement	FP EMC@
FP ESD requirement	FPESD@
TBT ESD requirement	BL_ESD@ V
X4EAQTBOLO1	PG61A GH51H

Item (X4E) un-pop	BOM Structure
EMI require reserve	XEMI@
EMC require reserve	XEMC@
ESD require reserve	XESD@
RF require reserve	@RF@

Item (X76)	BOM Structure
OVrm-uPI Gen1	X76UPIGEN1@
OVrm-ON Gen1	X76ONGEN1@
VRAM-SAMSUNG	X76SAM@
VRAM-MICRON	X76MIC@

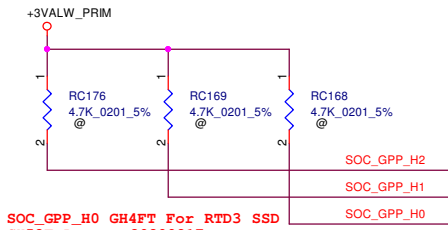
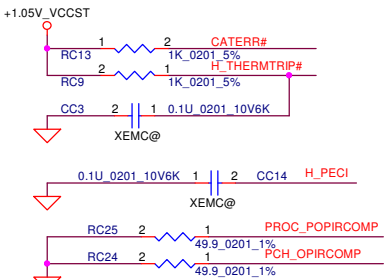
X76869BOL81 - UPI OVRM  
X76869BOL82 - ON OVRM  
X76869BOL83 - SAMSUNG  
X76869BOL84 - MICRON

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SOC\_GPP\_H0 GH4FT For RTD3 SSD  
GH52T Remove 20200817

SOC\_GPP\_H2  
BOOT STRAP1 - BIT3  
This is bit 1 of a total of 4-bit encoded pin straps for boot configuration.  
Refer to Boot Strap 0 (on GPP\_C5) for the encoding.  
INTERNAL PD 20K

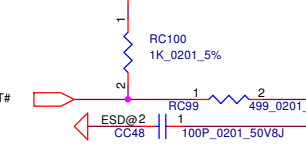
SOC\_GPP\_H1  
BOOT STRAP1 - BIT2  
This is bit 1 of a total of 4-bit encoded pin straps for boot configuration.  
Refer to Boot Strap 0 (on GPP\_C5) for the encoding.  
INTERNAL PD 20K

SOC\_GPP\_H0  
BOOT STRAP1 - BIT1  
This is bit 1 of a total of 4-bit encoded pin straps for boot configuration.  
Refer to Boot Strap 0 (on GPP\_C5) for the encoding.  
INTERNAL PD 20K

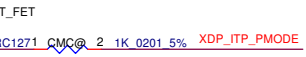
SOC\_WWAN\_RST# (No used)  
This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.  
INTERNAL PD 20K

CHECK power net name, 12/13

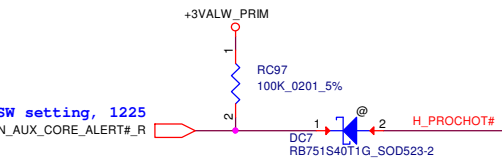
+1.05VS\_VCCSTG\_OUT\_LGC\_TERM



check SW setting for leakage, 1225

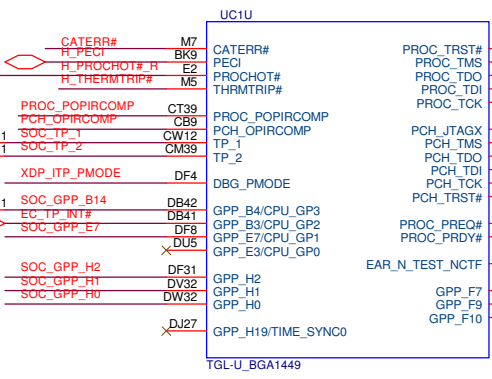


XDP\_ITP\_PMODE  
DFX TEST MODE  
INTERNAL PU 20K  
This strap should sample high. There should NOT be any on-board device driving it to opposite direction during strap sampling.

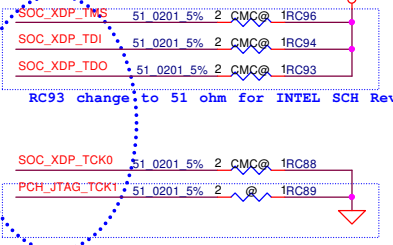


check SW setting, 1225

<17,44> VCCIN\_AUX\_CORE\_ALERT#\_R



Stall reset sequence after PCU PLL lock until de-asserted:  
1 = (Default) Normal Operation; No stall.  
0 = Stall.



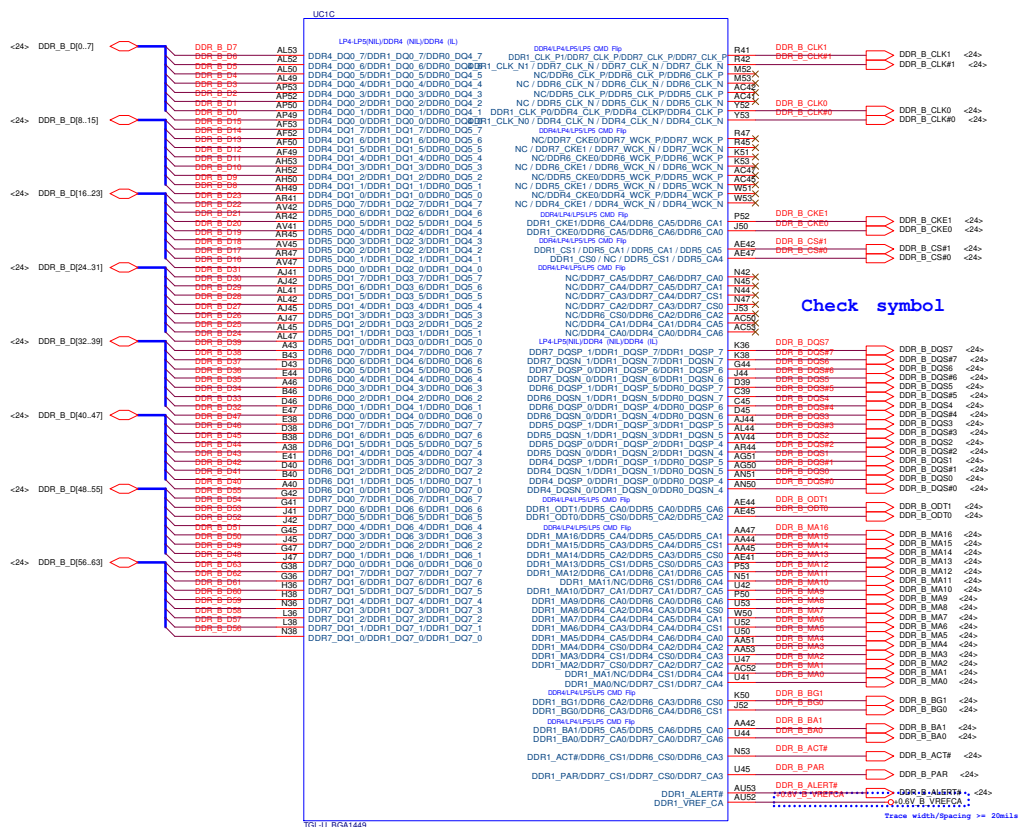
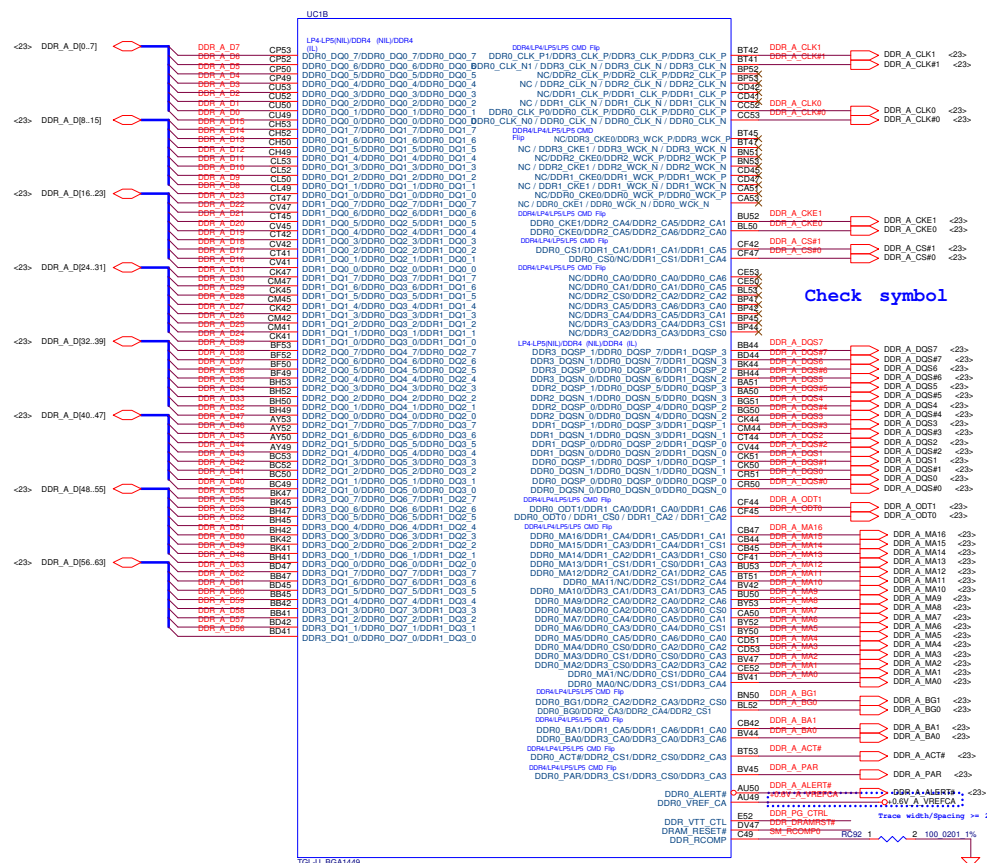
EDS 12.12 internal PH/PD

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				TGL-UP3(1/14)DDLMSIC,XDP		
				Size	Document Number	Rev
				LA-L051P		
				Date:	Wednesday, January 06, 2021	Sheet 7 of 121

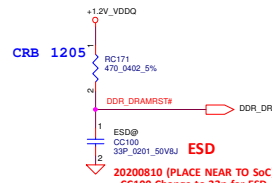
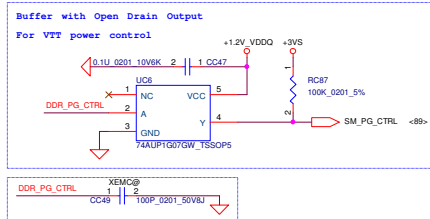


## Follow Intel DDR4 N1

DDR4: Refer to 609003\_TGL\_U\_DDR4\_SODIMM\_RVP\_SCH\_REV0p5

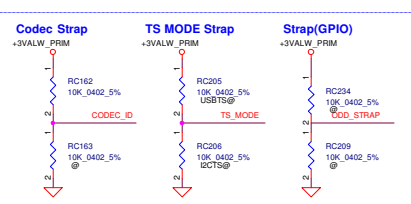
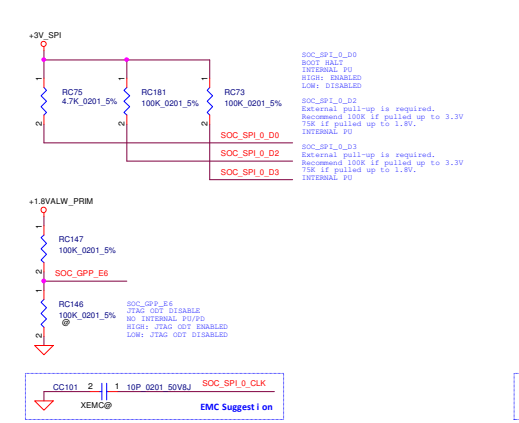


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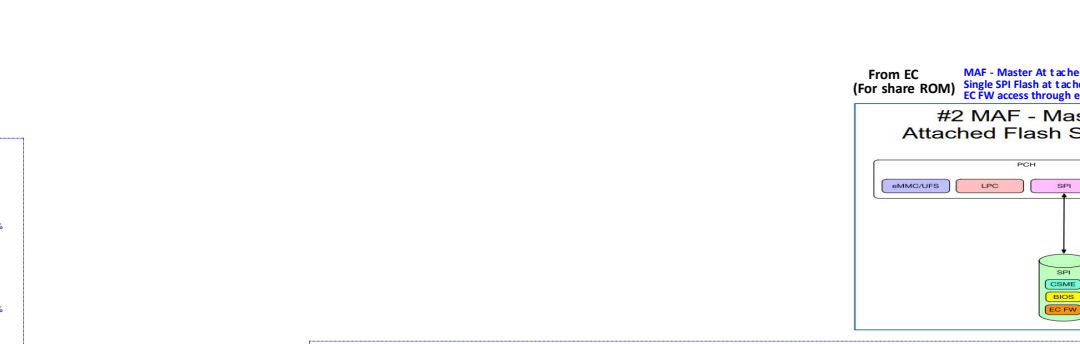
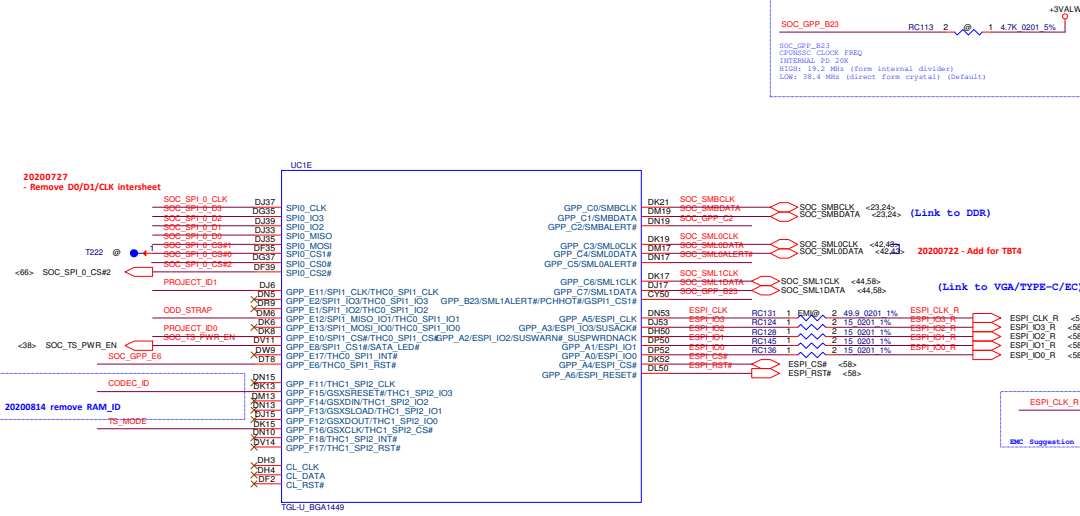
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Issued Date		Deciphered Date		Size	
2019/08/20		2020/12/31		TGL-UP3(3/14)DDR4	
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				1.0	
Date:				Wednesday, January 06, 2021	
				Sheet 8 of 121	





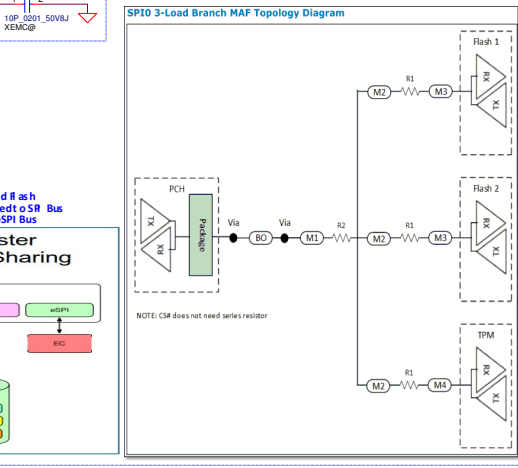
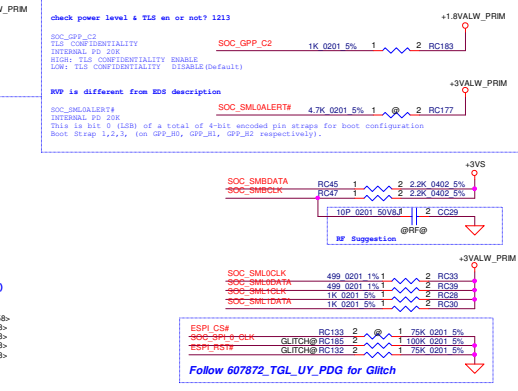
	Project_ID1	Project_ID0	PartNumber - Description
TBD	0	0	TBD
TBD	0	1	TBD
TBD	1	0	TBD
TBD	1	1	TBD

## 20200813 remove Memory Down Strap



Topology	BOM Conf ig
32M	1LD@
32M+TPM	2LD@+2LDTMP@

## 20200813 remove Memory Down Strap



Topology	BOM Conf ig
32M	1LD@
32M+TPM	2LD@+2LDTMP@

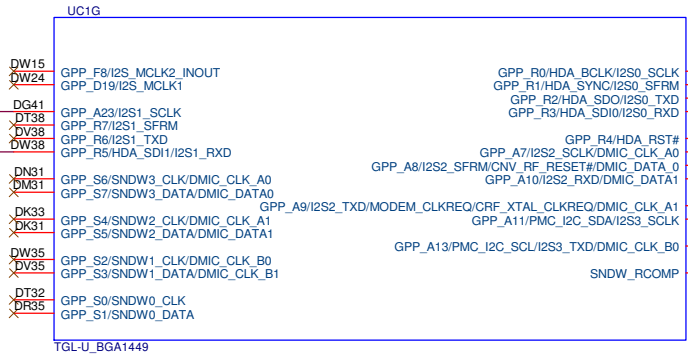
## 20200813 remove Memory Down Strap

20200722 - Add for TBT4  
<42,43,44> SOC\_DG\_BB\_FORCE\_PWR\_R

RC218 1 33 0201 5%

SOC\_DG\_BB\_FORCE\_PWR

HDA\_SDIN1



DR38 HDA\_BIT\_CLK  
DU37 HDA\_SYNC  
DT37 HDA\_SDOUT  
DV37 HDA\_SDIN0

DV41 HDA\_RST#  
DL53 PCH\_DMIC\_CLK  
DG51 PCH\_DMIC\_DATA  
DG50

PCH\_DMIC\_CLK <56>  
PCH\_DMIC\_DATA <56>  
DMIC

DL49 CLKREQ\_CNV#  
DL52

CLKREQ\_CNV# <52>

DH49 SOC\_BT\_ON R64 1

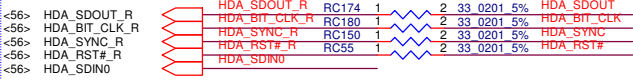
2 0 0402 5% BT\_ON <52>

DF33 SNDW\_RCOMP RC48 1

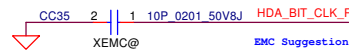
2 200 0201 1%

### HDA for AUDIO

20200819  
- Remove RC180 BOM config, must pop of PDG



Follow  
607872\_TGL\_UY\_PDG for Glitch



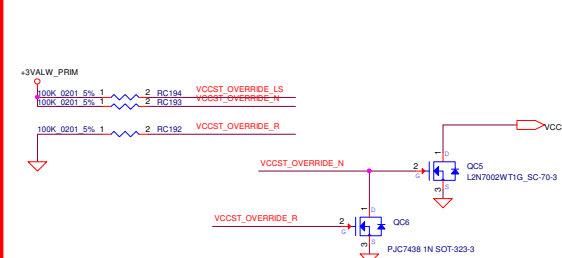
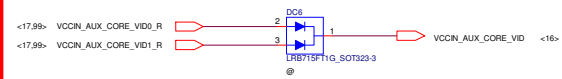
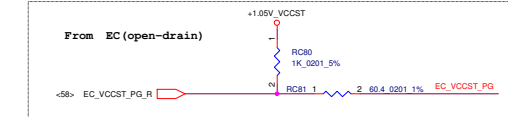
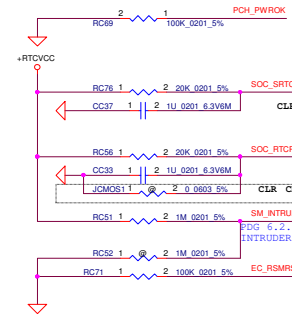
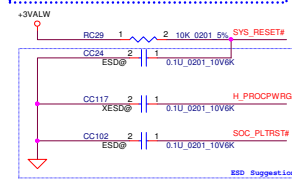
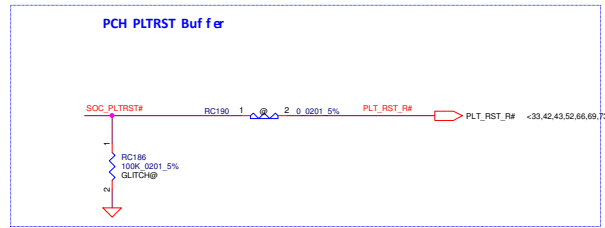
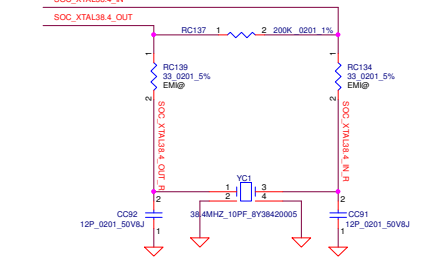
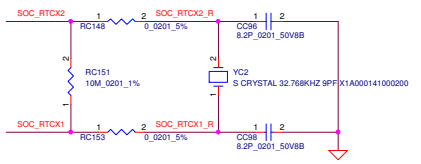
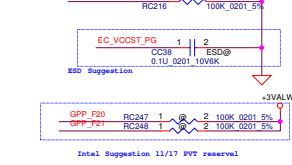
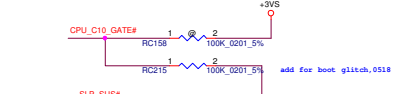
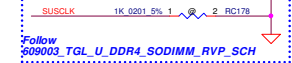
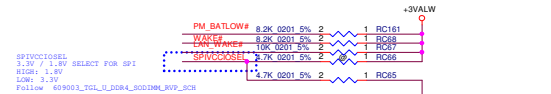
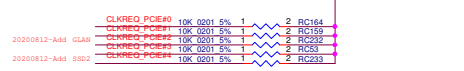
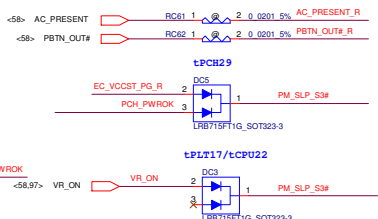
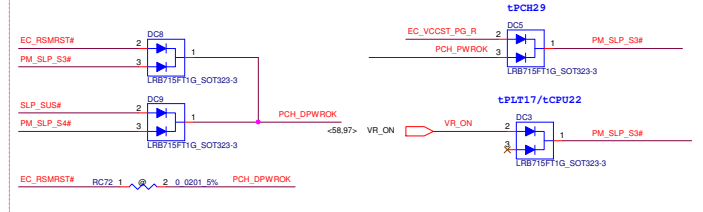
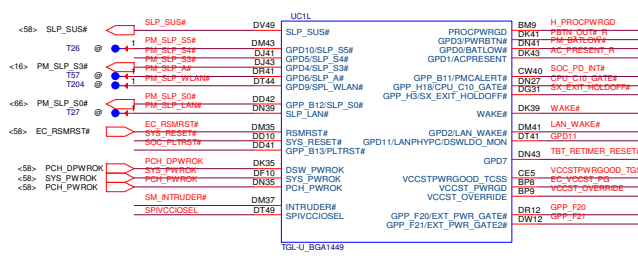
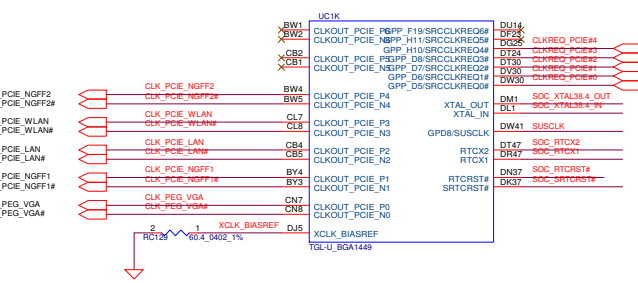
### To Enable ME Override

HDA\_SDOUT  
FLASH\_DESCRIPTOR SECURITY OVERRIDE  
INTERNAL PD 20K  
HIGH: OVERRIDEN  
LOW: SECURITY MEASURES NOT OVERRIDEN (DEFAULT)

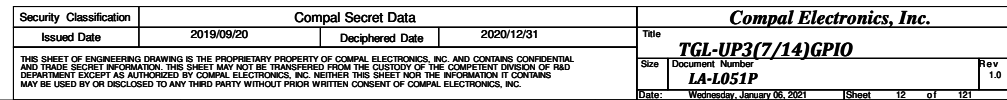
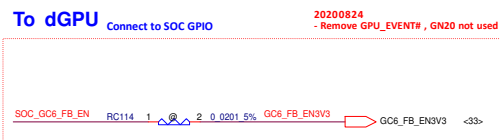
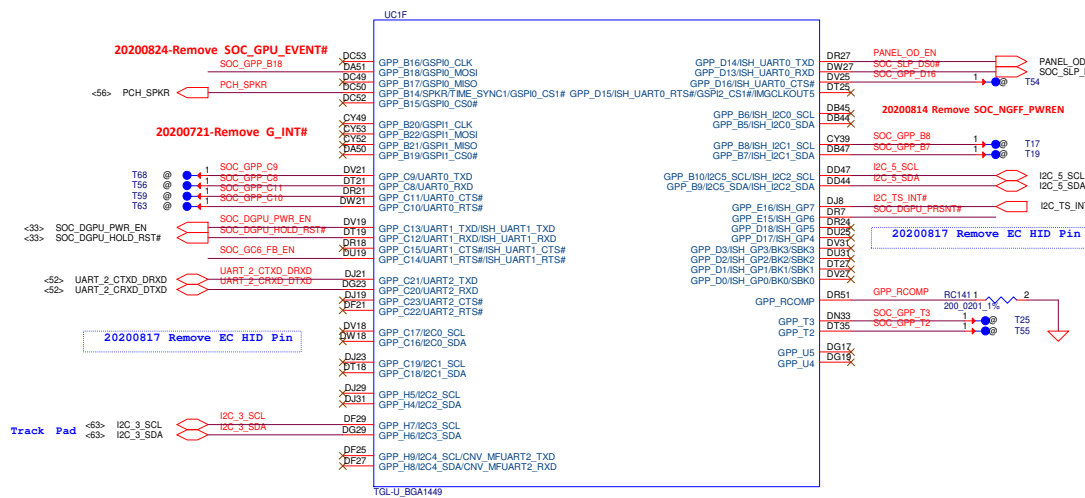


572631\_ICL\_PCH\_LP\_EDS\_Vol\_1\_Rev\_0p7  
VCCPGPFR: Audio Power 3.3V, 1.8V, or 1.5V  
Need to sync with codec VDDIO

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						Size		Document Number		Rev	
								LA-L051P		1.0	
Date:						Wednesday, January 06, 2021		Sheet 10 of 121			

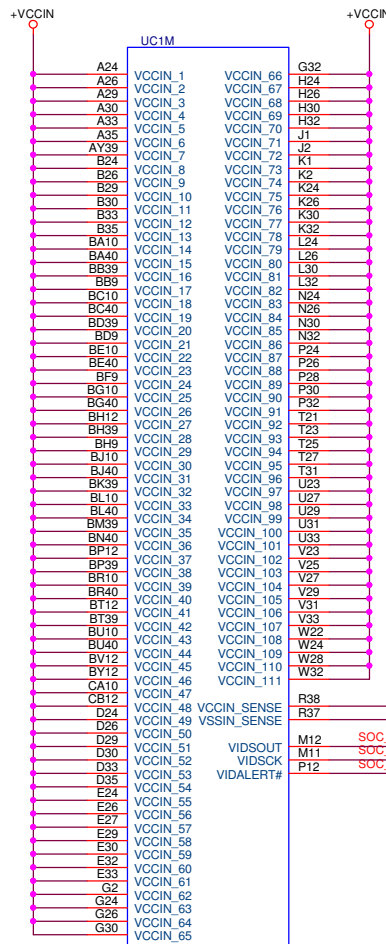
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				Date:	Wednesday, January 08, 2020	
				LA-10S1P		









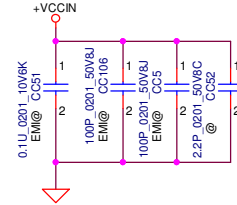
VCC\_SENSE\_VCCIN <97>  
VSS\_SENSE\_VCCIN <97>

M12 SOC\_SVID\_DAT  
M11 SOC\_SVID\_CLK  
P12 SOC\_SVID\_ALERT#

TGL-U\_BGA1449

### Package size?

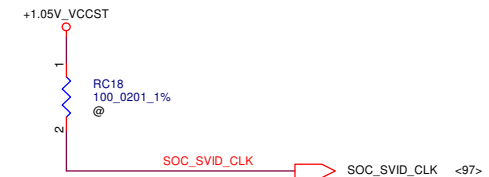
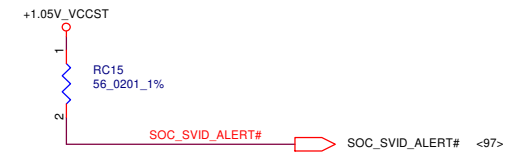
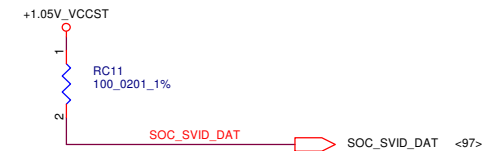
EMC CAPS-PLACE  
< 5mm from SOC VCCIN



### SVID DATA

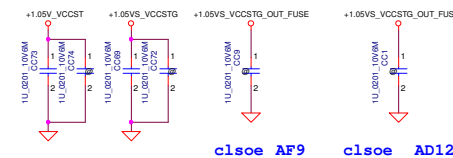
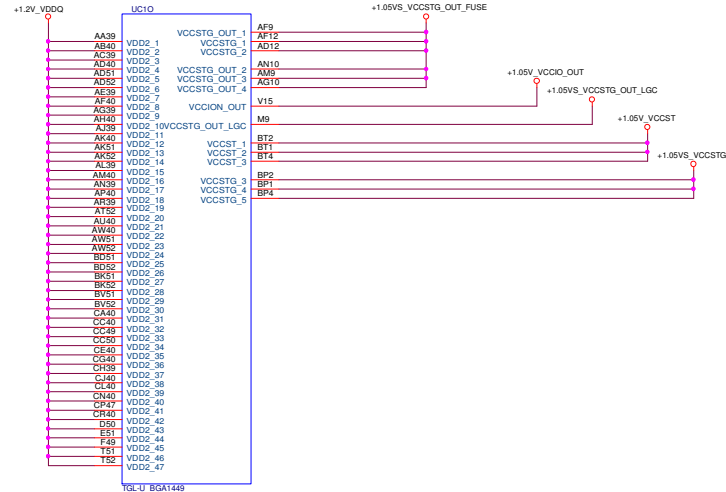
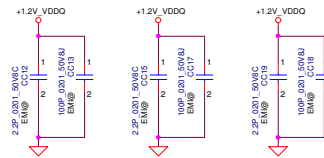
### SVID ALERT

### SVID CLOCK

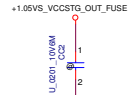


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				Size	Document Number	Rev
					LA-L051P	1.0
				Date: Wednesday, January 06, 2021		
				Sheet	15	of 121

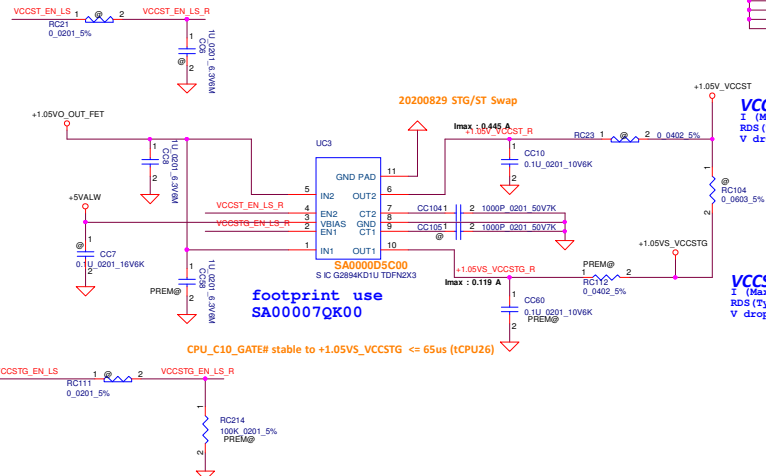




close AF9      close AD12



also AN10



**VCCST**  
I (Max) : 0.455 A(+1.05V\_VCCST)  
RDS(Typ) : 3.5 mohm  
V drop : 0.0016V

**VCCSTG**  
I (Max) : 0.119 A(+1.05VS\_VCCSTG)  
RDS(Typ) : 3.5 mohm  
V drop : 0.0004V

```
Place on CPU Side
1uF* 10
10uF* 16
47uF * 2
```

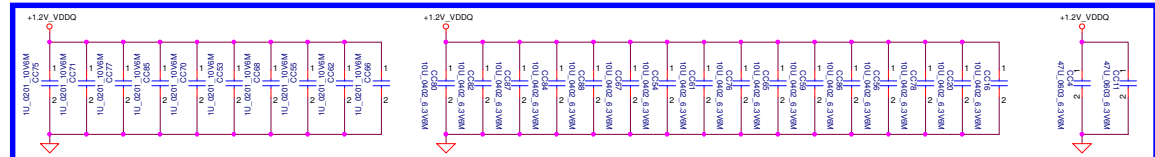
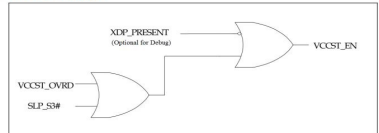
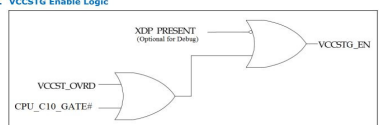


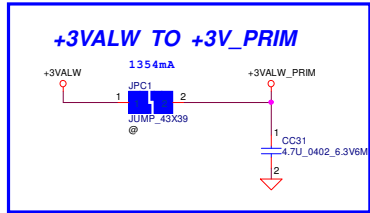
Figure 231. VCCST Enable Logic



**Figure 232. VCCSTG Enable Logic**

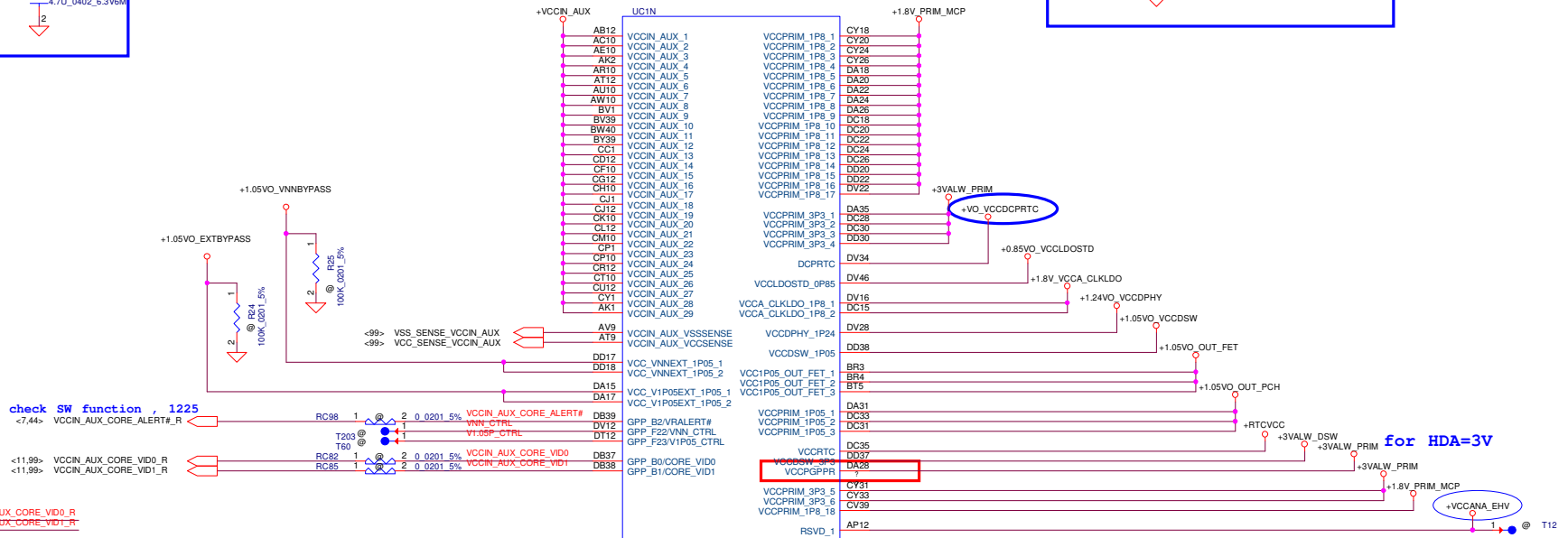
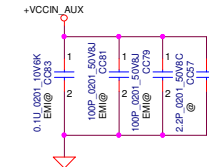


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Date:				Wednesday, January 06, 2021	Sheet 16 of 121

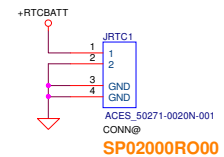
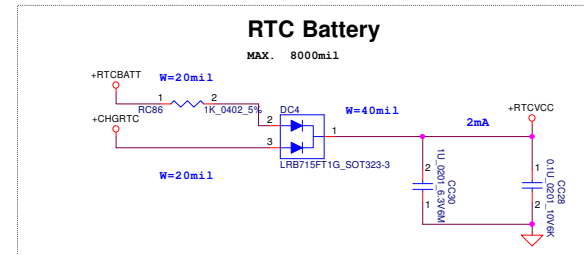


Package size?

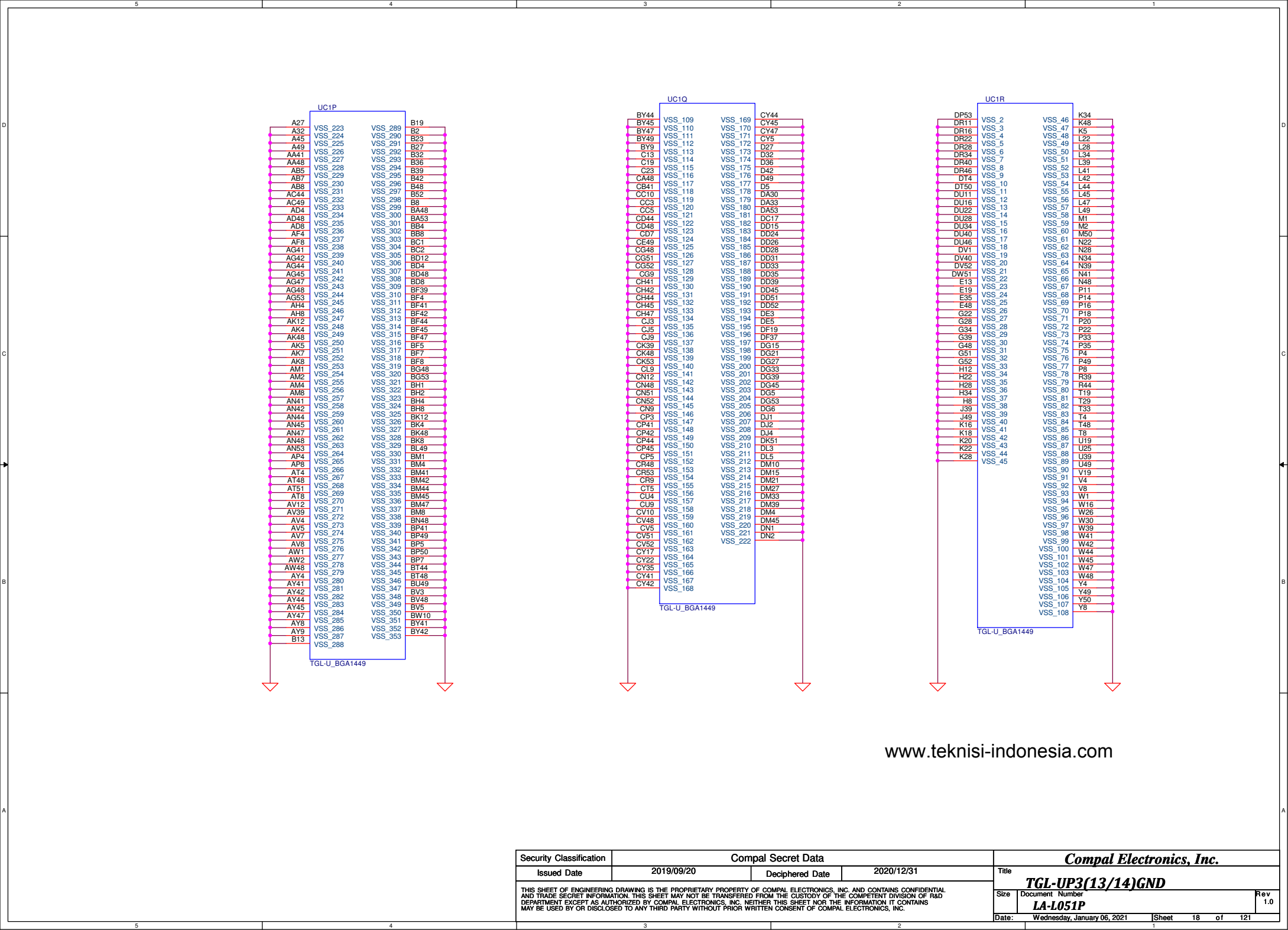
EMC CAPS-PLACE  
< 5mm from SOC VCCIN\_AUX



NOTE:  
576591-tgl-pch-lp-ads-vollof2-rev0p5  
VCCPGPPR: Audio Power 3.3V, 1.5V, or 1.5V  
Need to sync with codec VDDIO.  
607872\_TGL\_UY\_PDG\_Rev0p5  
When configured as 3.3V or 1.8V, VCCPGPPR can be merged directly with  
either VCCPRIM\_1P8 or VCCPRIM\_3P3 depending on their operating voltage.



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				LA-1051P	Rev 1.0
				Date: Wednesday, January 06, 2021	Sheet 17 of 121

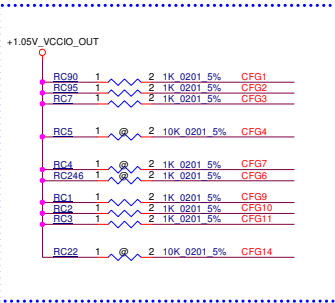


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								Size		Document Number		Rev	
								LA-L051P				1.0	
								Date:		Wednesday, January 06, 2021		Sheet 18 of 121	

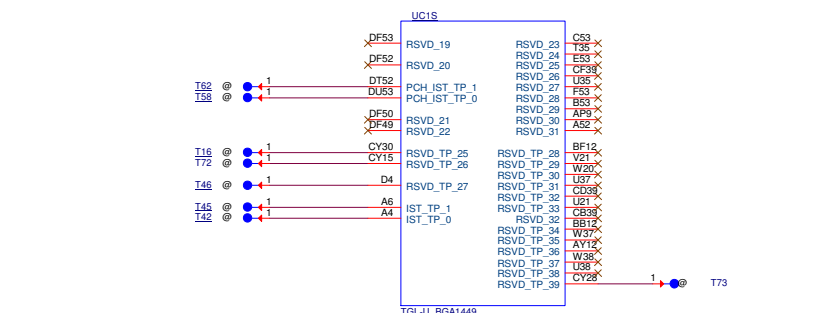
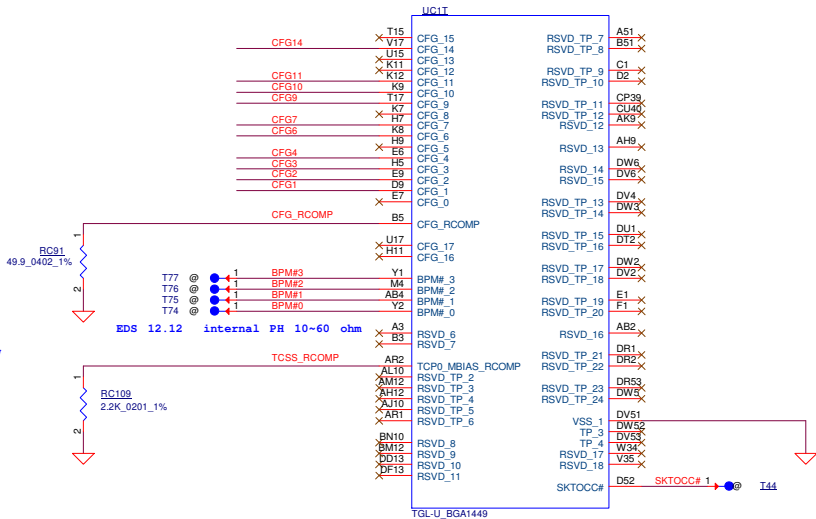
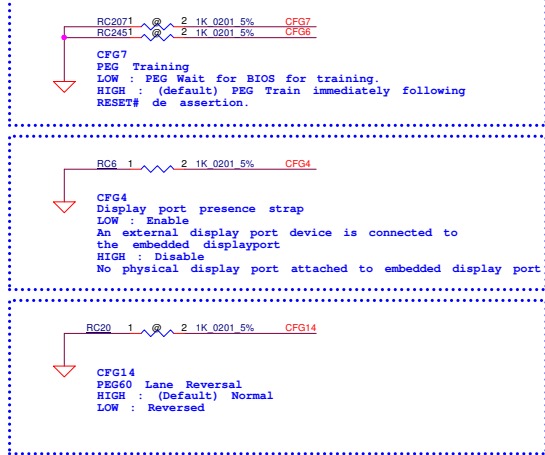
CFG	Description	Termination	Resistor
	Operation; No stall. - 0 = Stall		
CFG[0]	RSVD	None	
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled, - 0 = Enabled.	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: - 1 - (Default) Normal - 0 - Reversed	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[17:15]	RSVD	None	

CFG Signals have int. PH 3K ohm.



CFG Signals  
(For Strap & XDP)

20200902  
- RC4 change to 1k (CFG7) for PDG2.0 update  
- Add RC246, 1K, PH & RC245, 1K, PH, (CFG6), for PDG2.0 update & Intel SCR review



GH52T CPU QS



S IC FH8069004529905 OVBA B1 2.8G BGA 171165QS@ SA0000DRG30

MP



S IC FH8069004531301 SRK05 B1 2.4G ABO I 511135MP@ SA0000DTU30

GH51H/71H CPU QS



S IC FH8069004600005 QWL2 B1 3.1G BGA S 5111300HQS@ SA0000E4710

MP



S IC FH8069004600005 SRKH6 B1 3.1G ABO I 5111300HMP@ SA0000E4730

S IC FH8069004599910 QWKW B1 3.3G BGA S 1711370HMP@ SA0000E4630



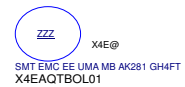
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PCB 3BQ LA1051P REV0 MB 4 S DAZ3BQ00100



HDMI LOGO RO000003HM

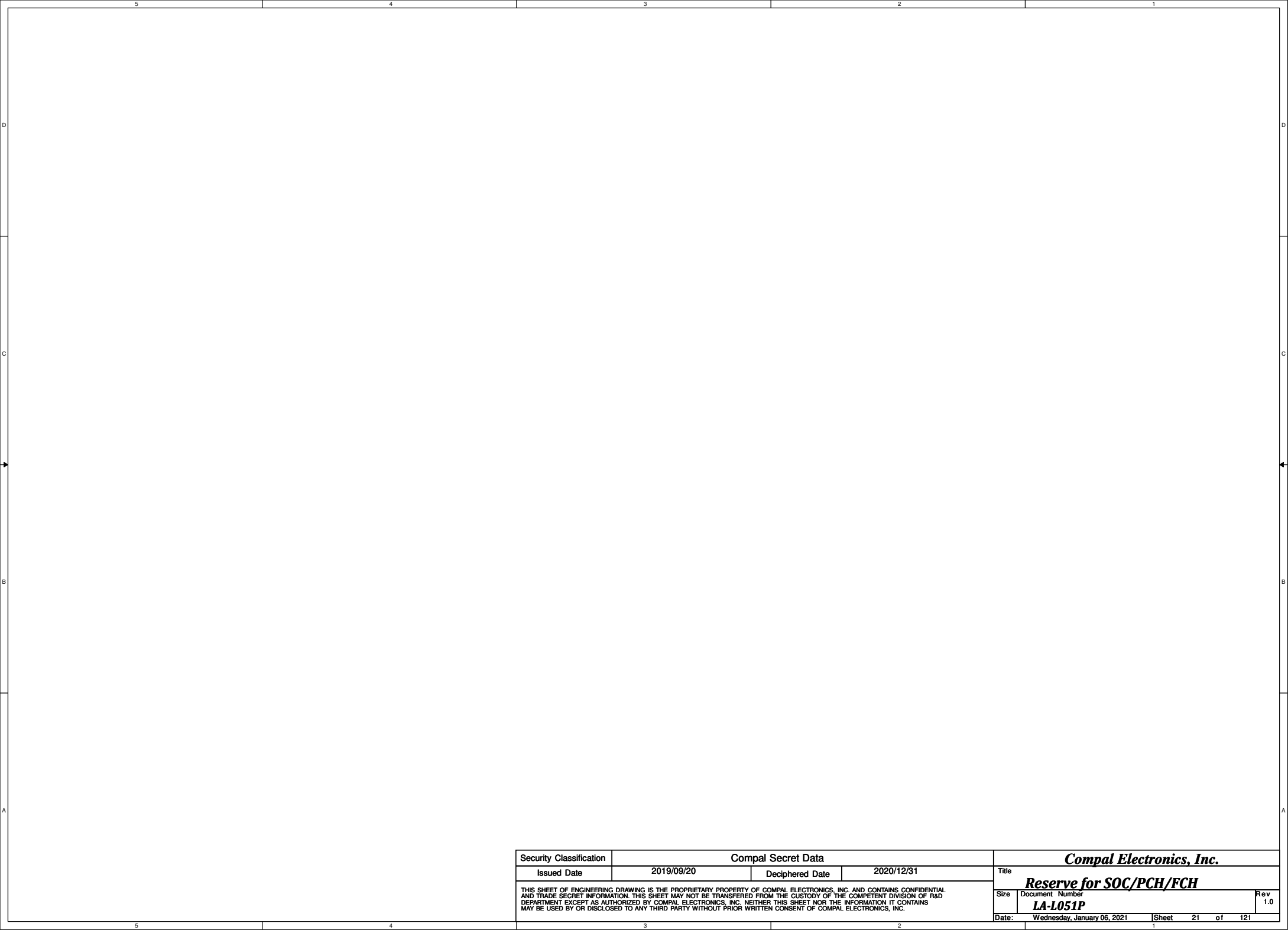


SMT EMC EE UMA MB AK281 GH4FT X4EAQTBOL01

Security Classification		Compal Secret Data		Title	
Issued Date	2019/09/20	Deciphered Date	2020/12/31	TGL-UP3(14/14)RSVD,CFG	
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				Sheet	19 of 121



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								Size		Document Number		Rev	
								LA-L051P				1.0	
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								Size		Document Number		Rev	
								LA-L051P		1.0			
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					Size	Document Number		Rev			
						LA-L051P		1.0			
					Date:	Wednesday, January 06, 2021		Sheet	22	of	121

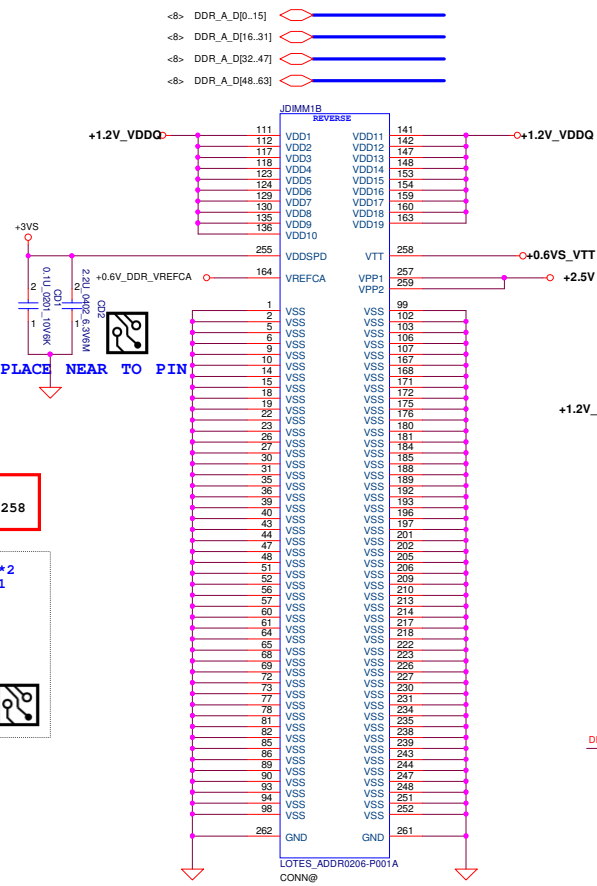
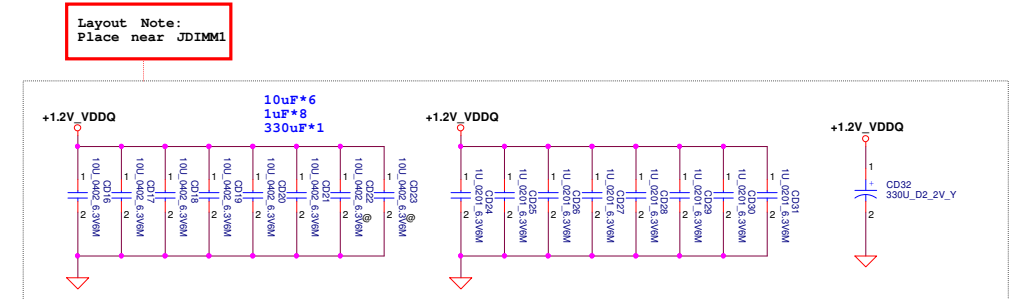
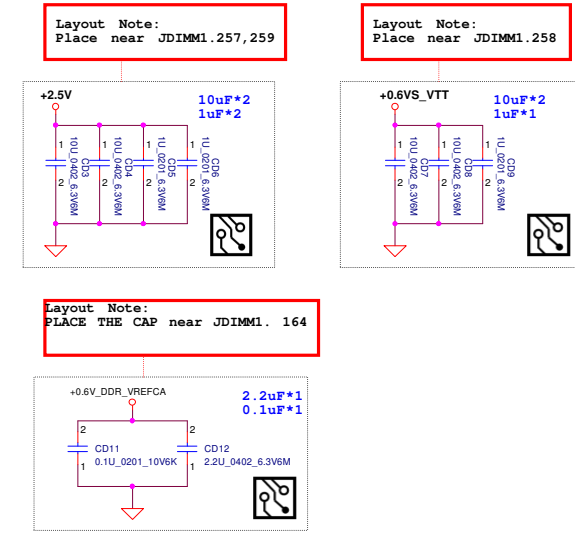


CHANNEL-A ( Interleaved Memory )

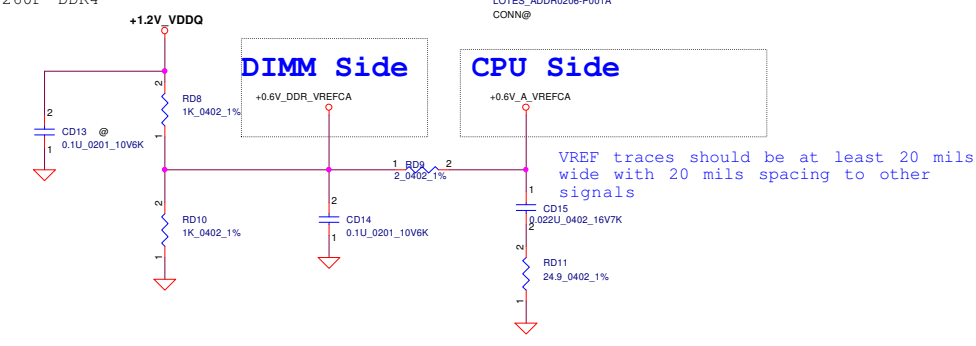
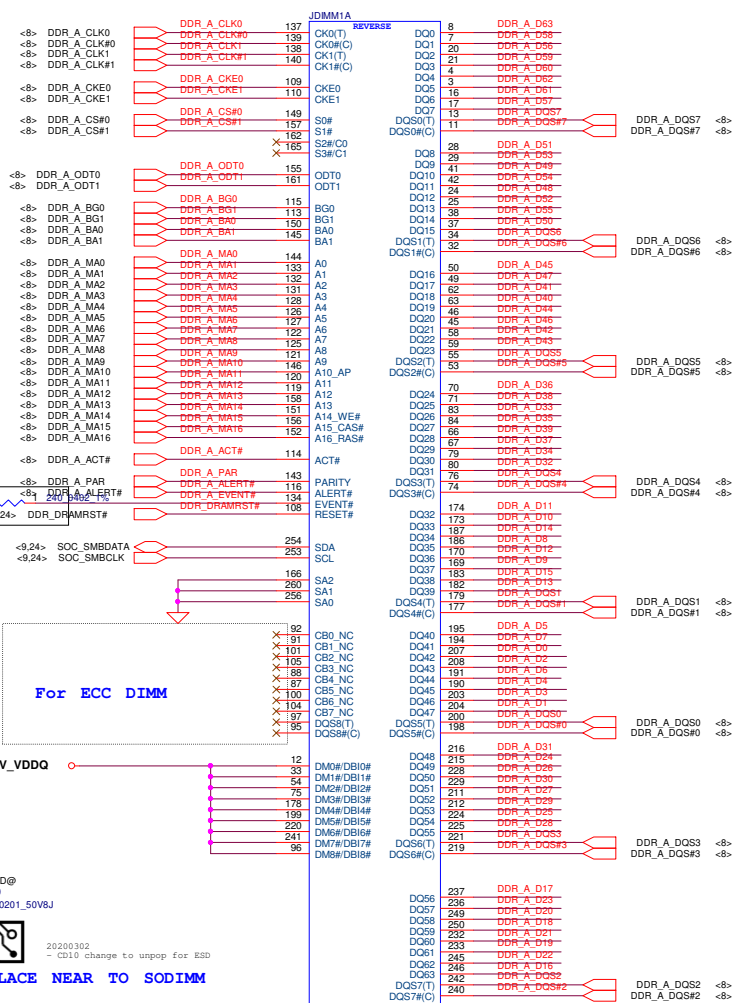
> BOT : Reverse type (4mm)

> Non-ECC SO-DIMM

SPD ADDRESS FOR CHANNEL A :  
WRITE ADDRESS: 0XA0  
READ ADDRESS: 0XA1  
SA0 = 0; SA1 = 0; SA2 = 0.  
DDR4 POR OPERATING SPEED: 1867 MT/S  
STRETCH GOAL IS 2133 MT/S

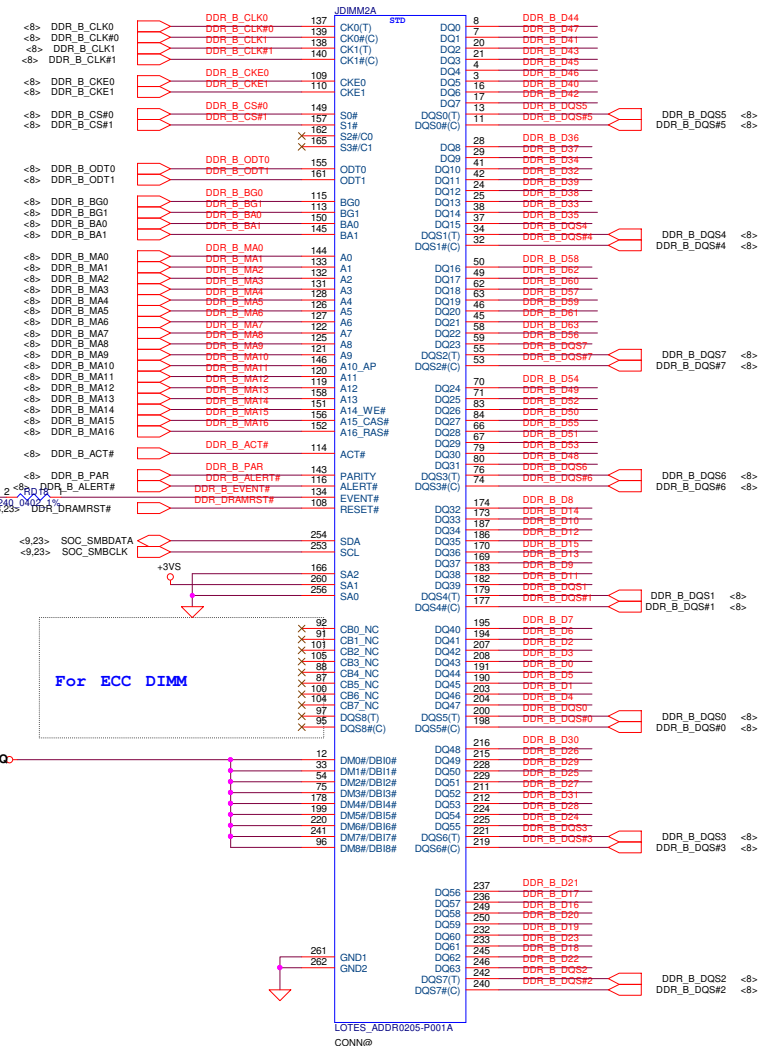


Part Number: SP07001CY00  
Part Value: S SOCKET LOTES ADDR0206-P001A 260P DDR4

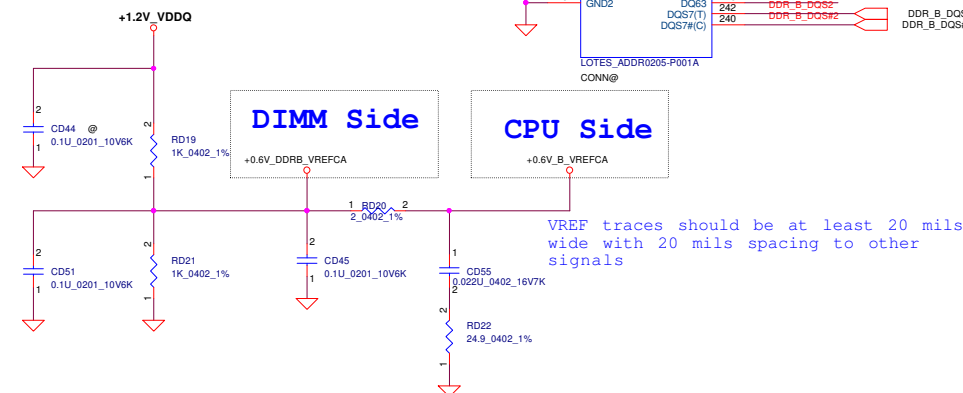


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Issued Date	2019/09/20	Deciphered Date	2020/09/20	Title	DDRIV_CHA: DIMM0
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Size	Document Number	LA-L051P		Date	Wednesday, January 06, 2021
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## > Non-ECC SO-DIMM



Part Number: SP07001HW00  
Part Value: S SOCKET LOTES ADDR0205-P001A DDR4 STD



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				Size	Document Number	Rev
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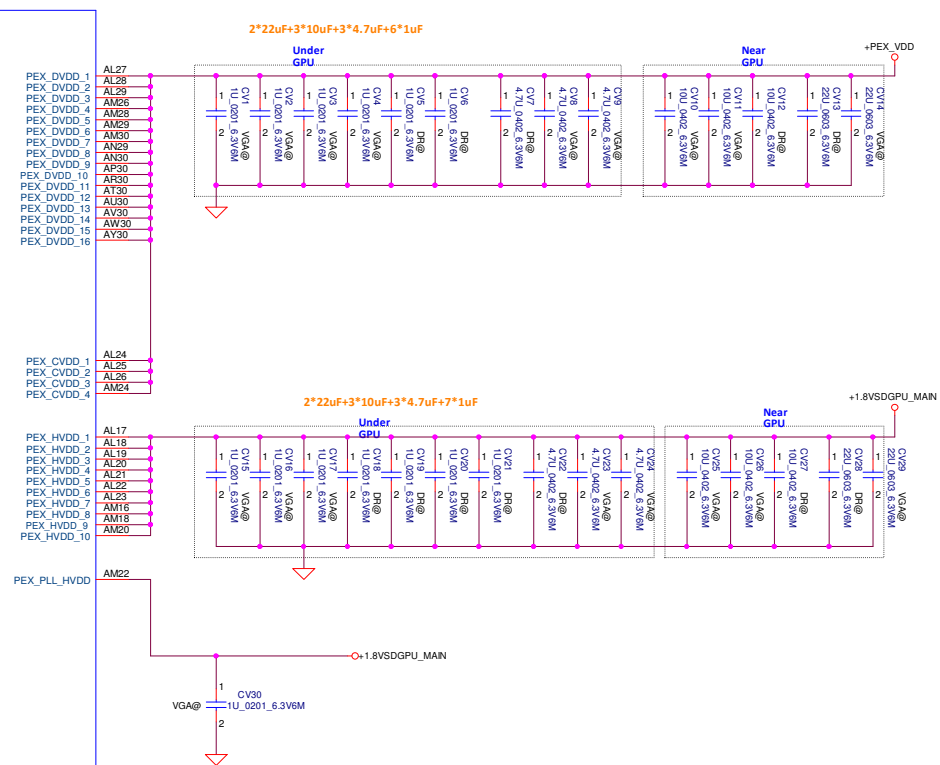
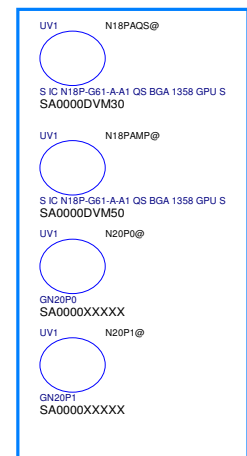
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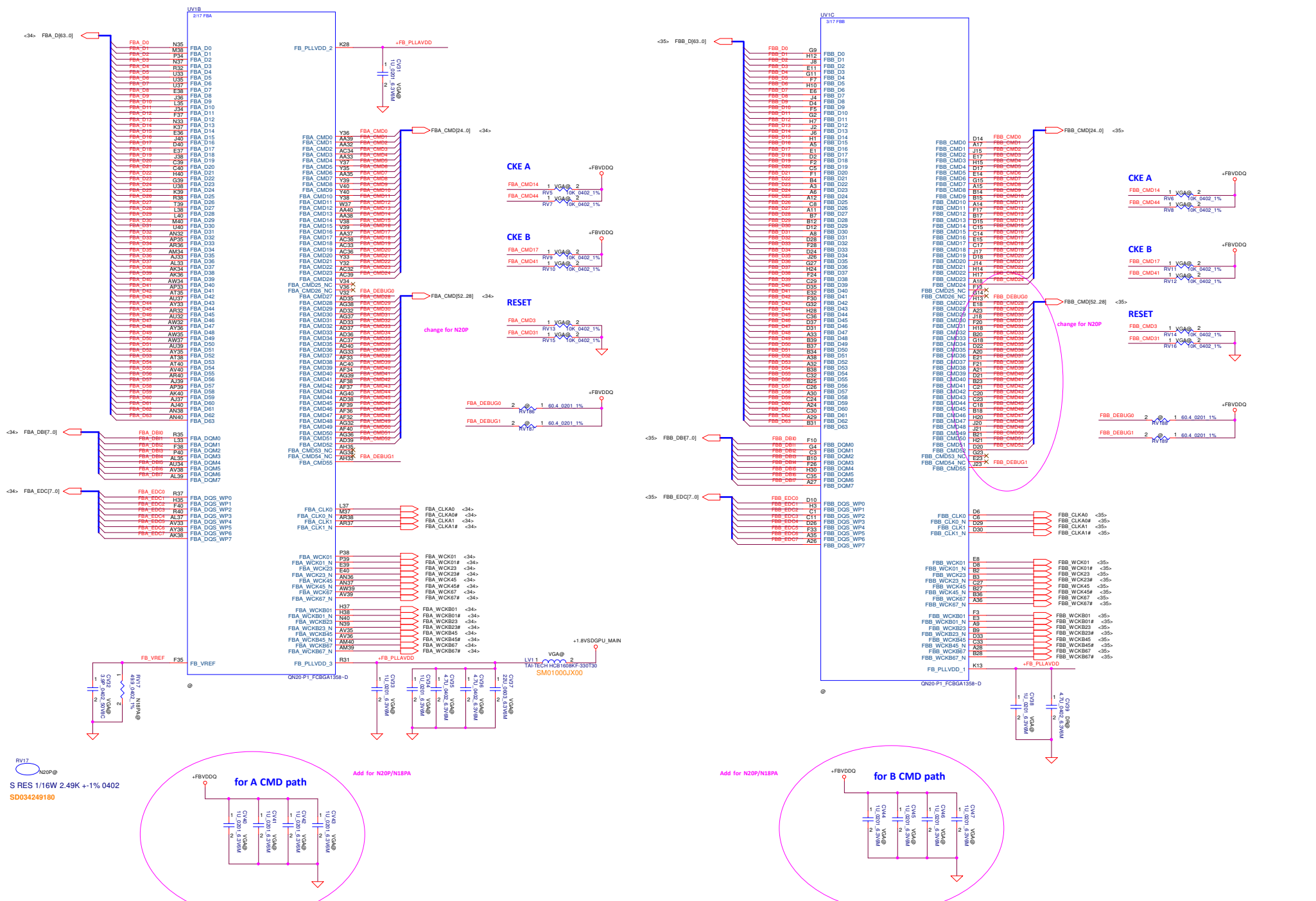
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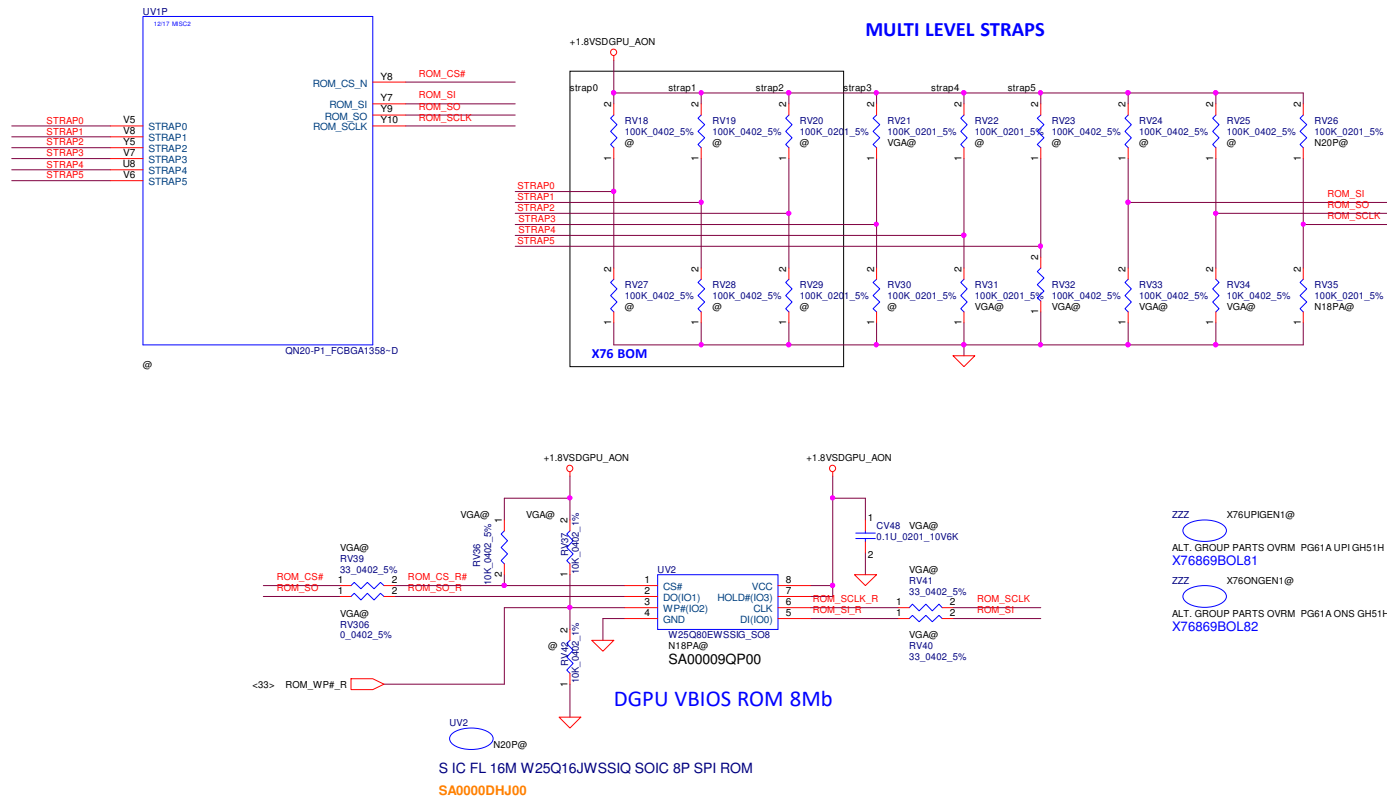
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To N18PG61A / N20P DGPU x 4 Lane







## N18PA

Table 11.3 RAMCFG

Strap Pins See Note			RAMCFG Setting Number	
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)	
L	L	L	0 (0x0000)	
L	L	H	1 (0x0001)	
L	H	L	2 (0x0002)	
L	H	H	3 (0x0003)	
H	L	L	4 (0x0004)	

Table 11.5 SMB ALT\_ADDR, DEVID\_SEL, PCIE\_CFG, VGA\_DEVICE

Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1

ROM_SO (10K)	ROM_SI	ROM_SCLK	Strap5	Strap4	Strap3	Strap2	Strap1	Strap0
L	L	L	L	L	H	RVL	RVL	RVL

SAMSUNG (000)	MICRON (001)	HYNIX (010)
RV27 100K_0402_5% SD028100380	RV15 100K_0402_5% SD028100380	RV27 100K_0402_5% SD028100380
RV28 100K_0402_5% SD028100380	RV16 100K_0402_5% SD028100380	RV19 100K_0402_5% SD028100380
RV29 100K_0201_5% SD043100380	RV20 100K_0201_5% SD043100380	RV22 100K_0201_5% SD043100380

## N20P

Table 9.3 RAMCFG

Strap Pins See Note			RAMCFG Setting Number	
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)	
L	L	L	0 (0x0000)	
L	L	H	1 (0x0001)	
L	H	L	2 (0x0002)	
L	H	H	3 (0x0003)	

Table 9.5 SMB ALT\_ADDR, DEVID\_SEL, PCIE\_CFG, VGA\_DEVICE

Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1

ROM_SO (10K)	ROM_SI	ROM_SCLK	Strap5	Strap4	Strap3	Strap2	Strap1	Strap0
L	L	H	L	L	H	RVL	RVL	RVL

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Date: Wednesday, January 06, 2021				Sheet	29 of 121



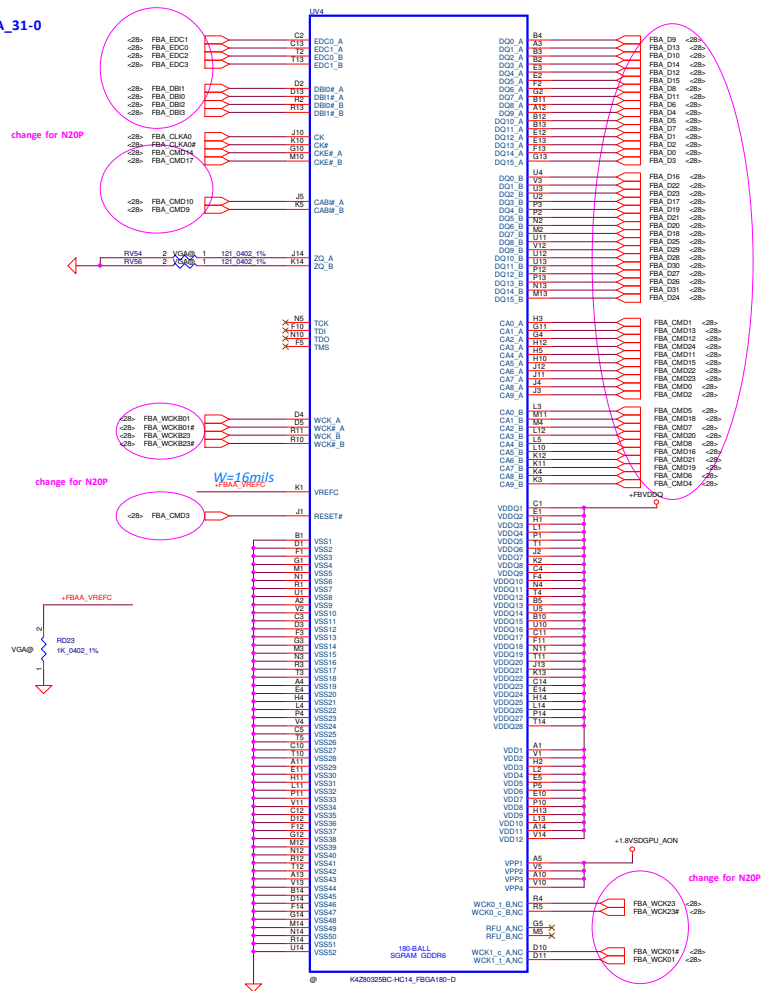




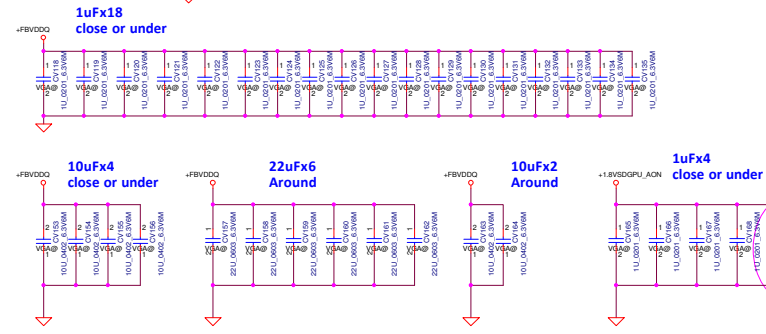
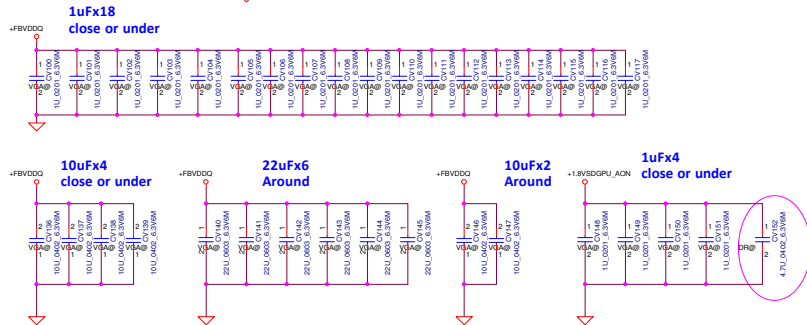
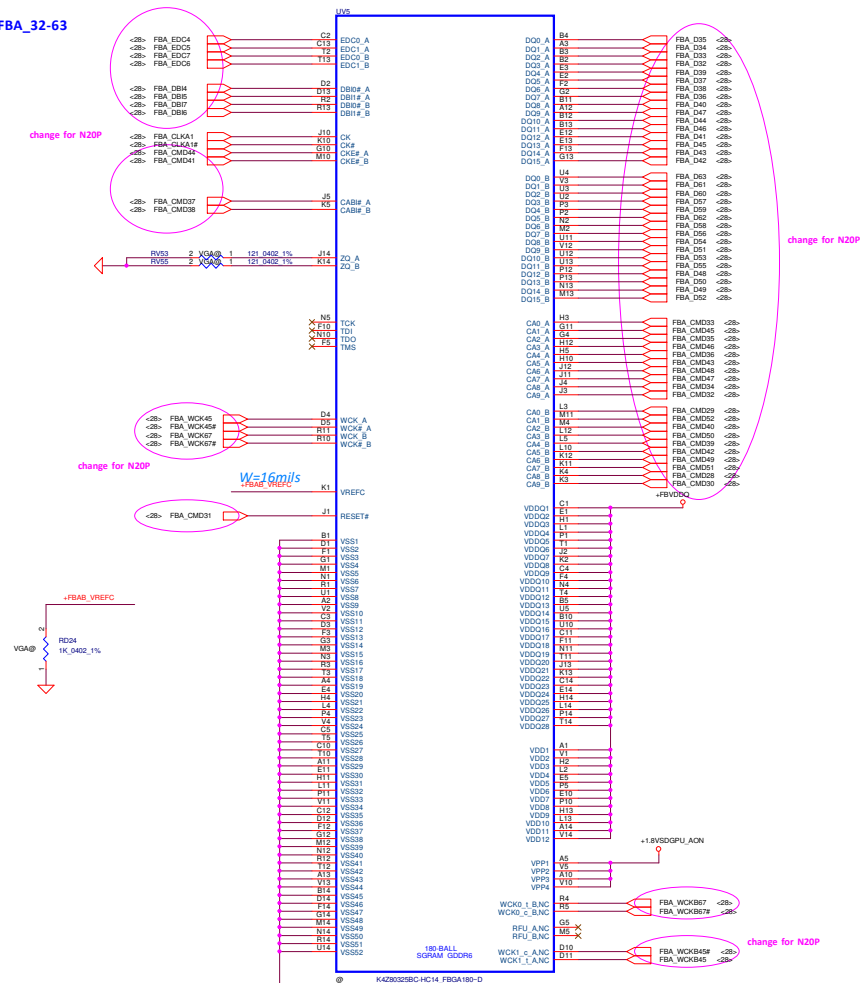


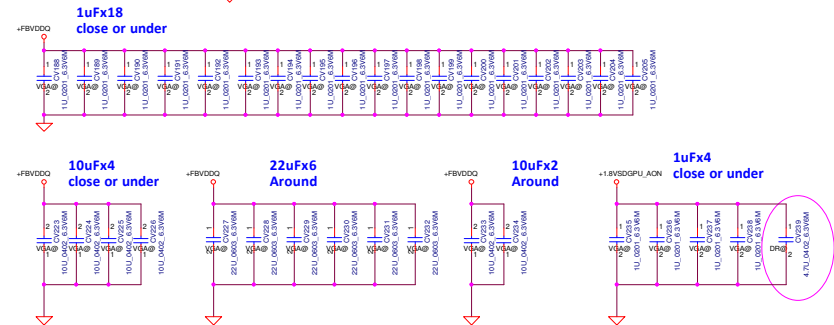
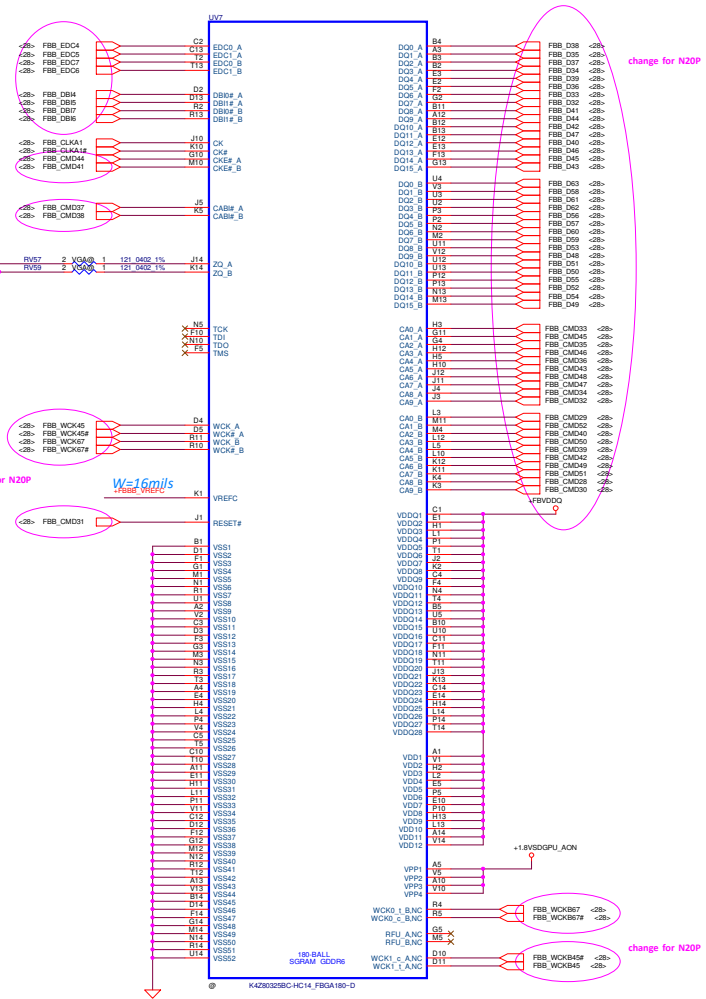
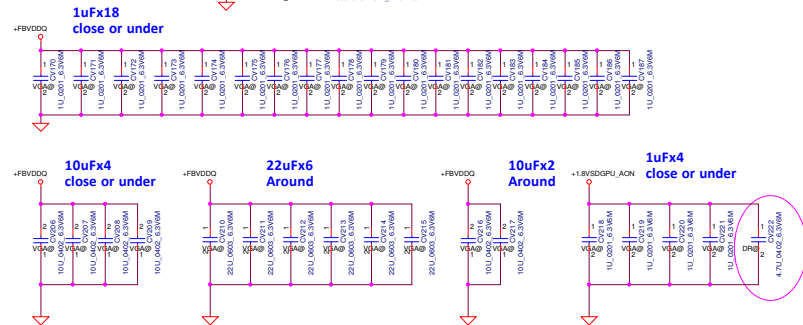
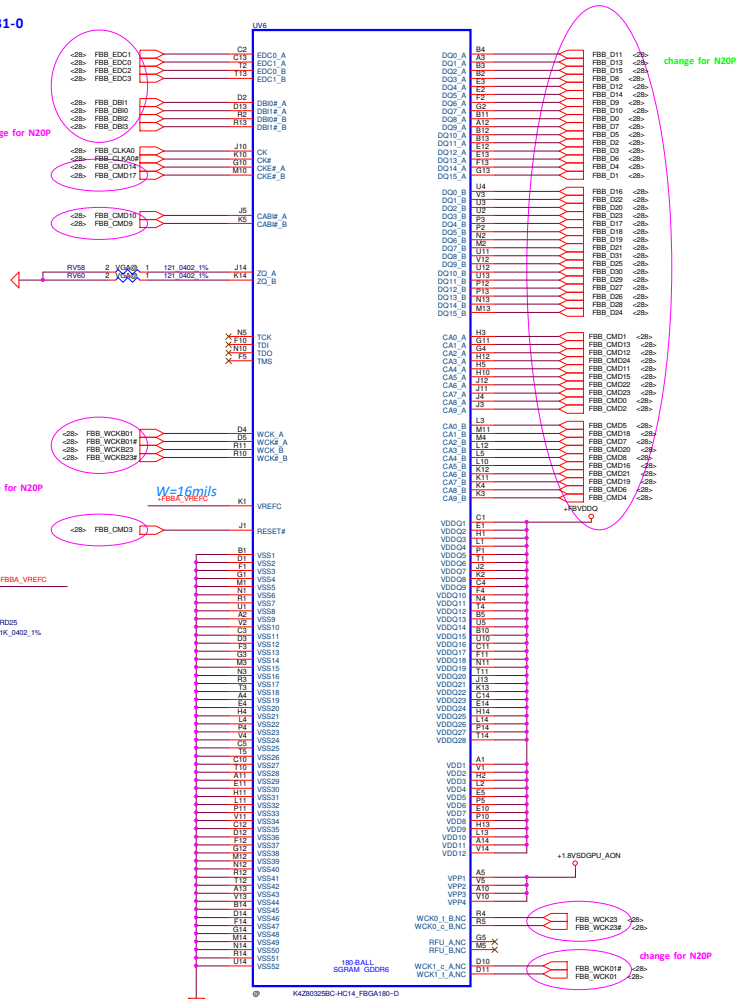


FBA\_31-0



FBA\_32-63



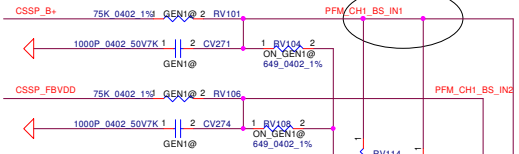


# GEN2 gain control by VBIOS

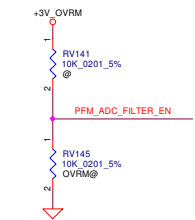
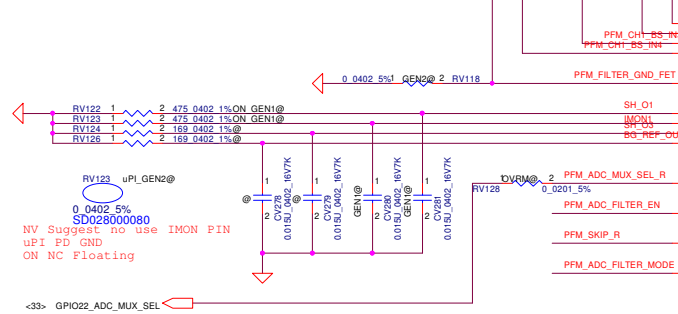
RV101 GEN2@  
0\_0402 5%  
SD028000080

RV106 GEN2@  
0\_0402 5%  
SD028000080

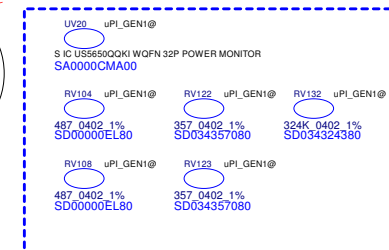
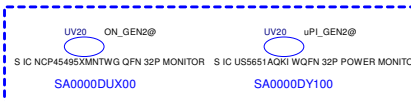
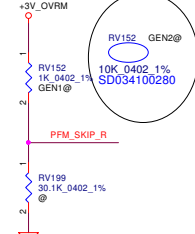
## NV Suggest



UPI-Semi suggest pop CV274/CV271 when GEN2  
Keep NV suggest to unpop when GEN2.

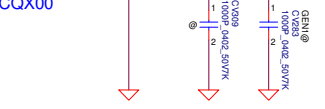
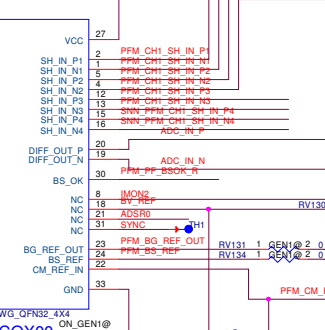
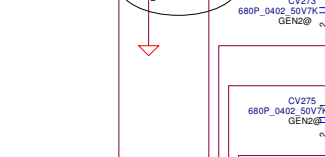


## NV Suggest



## For OVRM Keep ON

## NV Suggest



# GEN2 gain control by VBIOS

RV103 GEN2@  
0\_0402 5%  
SD028000080

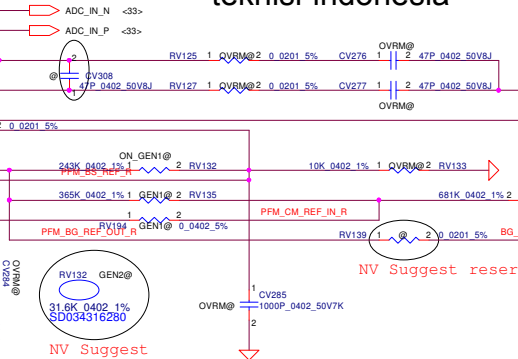
RV109 GEN2@  
0\_0402 5%  
SD028000080

# GEN2 gain control by VBIOS

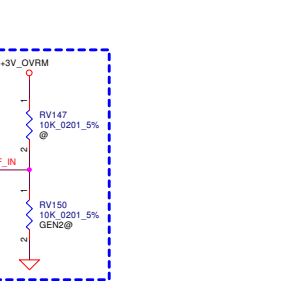
RV193 GEN2@  
0\_0402 5%  
SD028000080

RV192 GEN2@  
0\_0402 5%  
SD028000080

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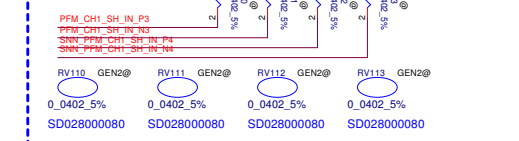
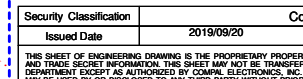
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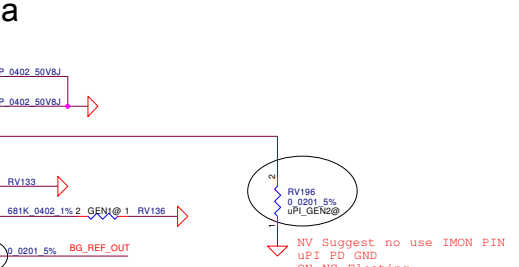
## NV Suggest



## NV Suggest



## NV Suggest



## NV Suggest



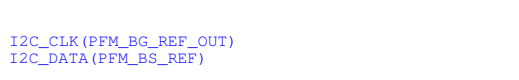
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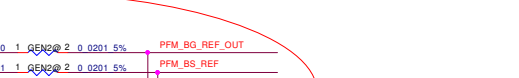
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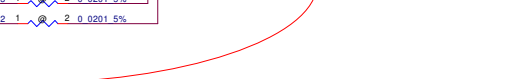
## NV Suggest



## NV Suggest



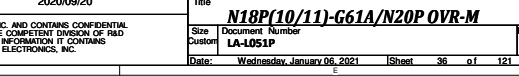
## NV Suggest



## NV Suggest



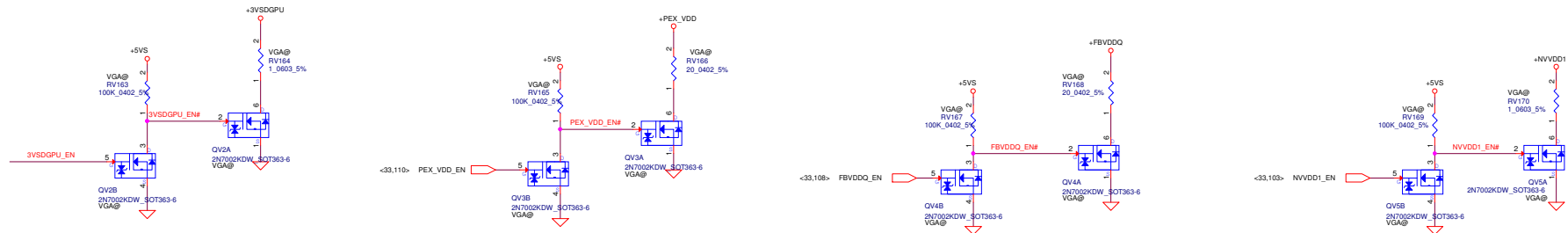
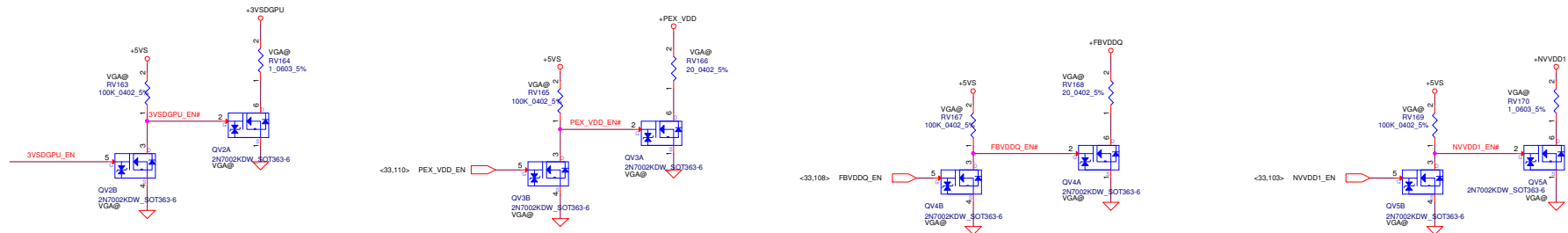
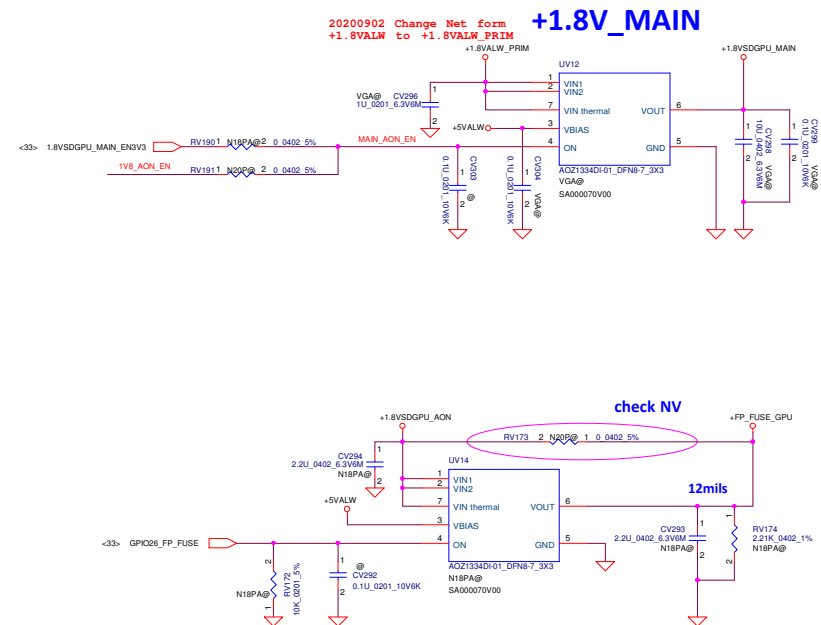
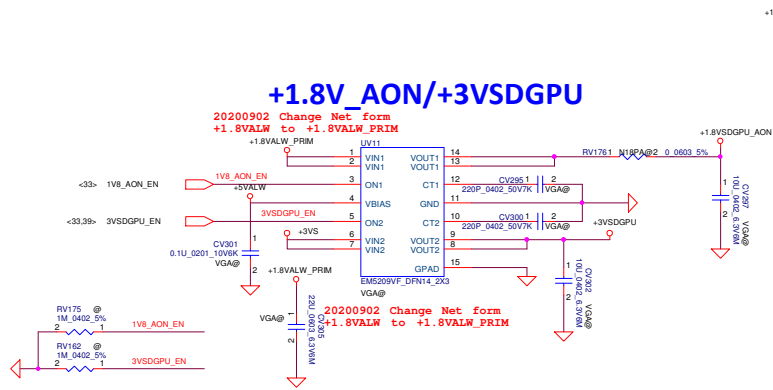
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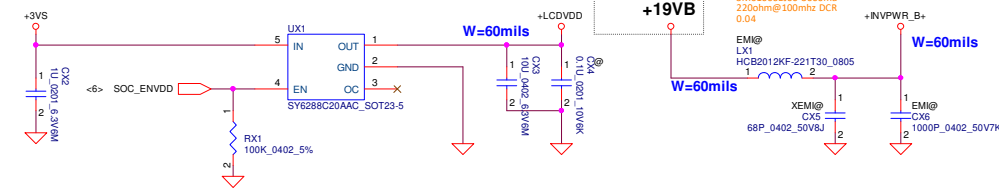
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Deciphered Date	2020/09/20
Title	Compal Electronics, Inc.
Size	118P(10/11)-G61A/N20P OVR-M
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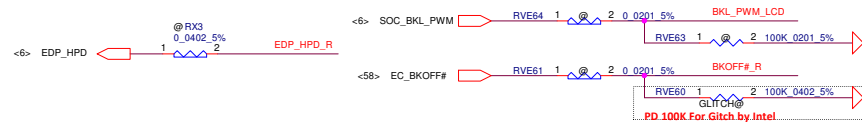




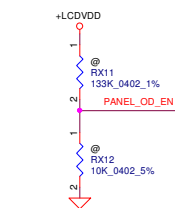
## LCD POWER CIRCUIT



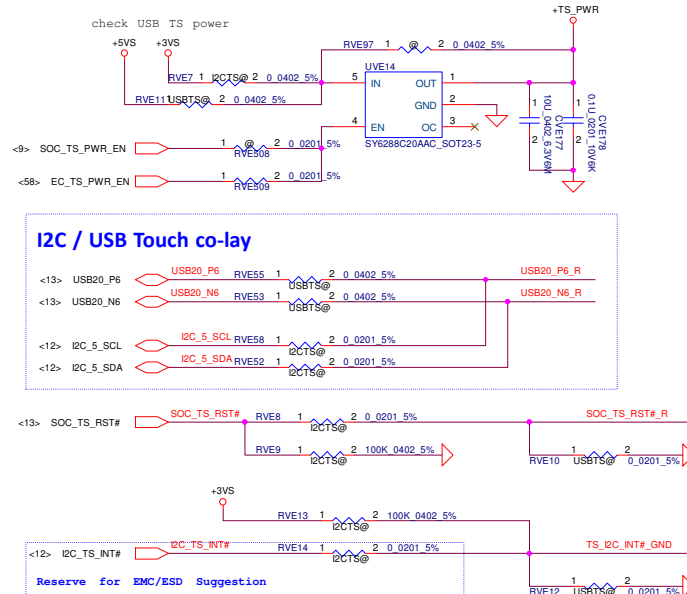
## LCD enable signal



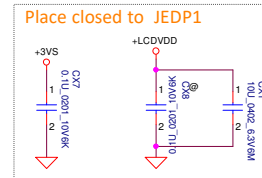
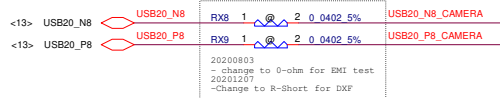
## Panel OD



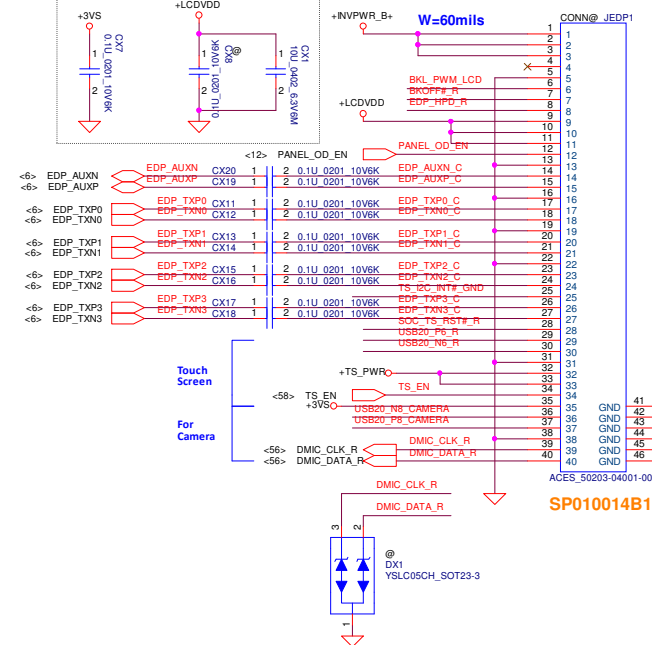
20190506  
- RX11 change to unpop  
- B105 needs to detect panel  
to select B or L.



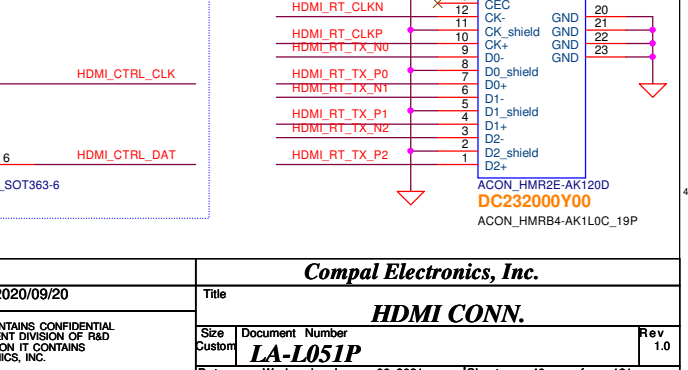
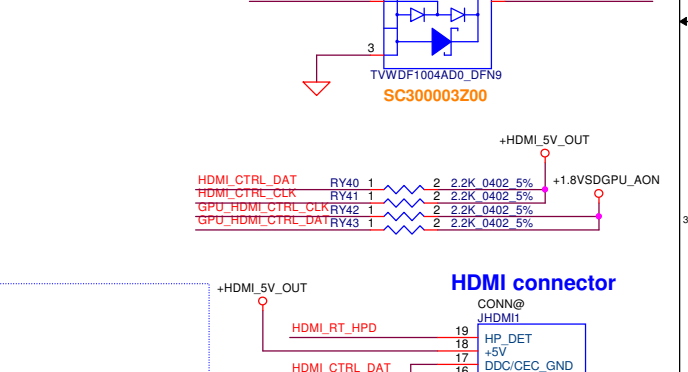
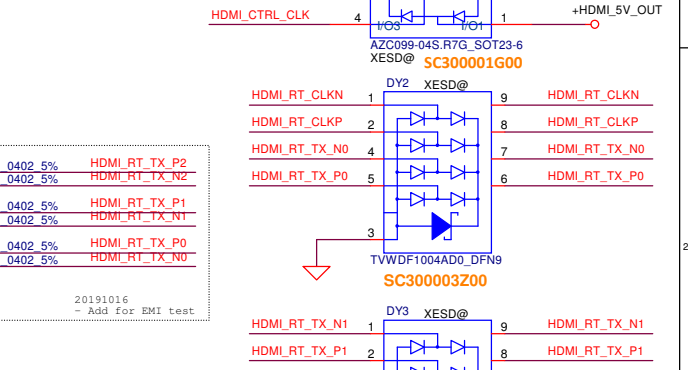
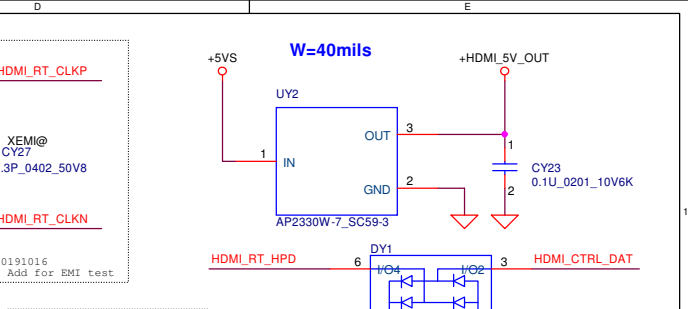
## CAMERA



## LED PANEL Conn.





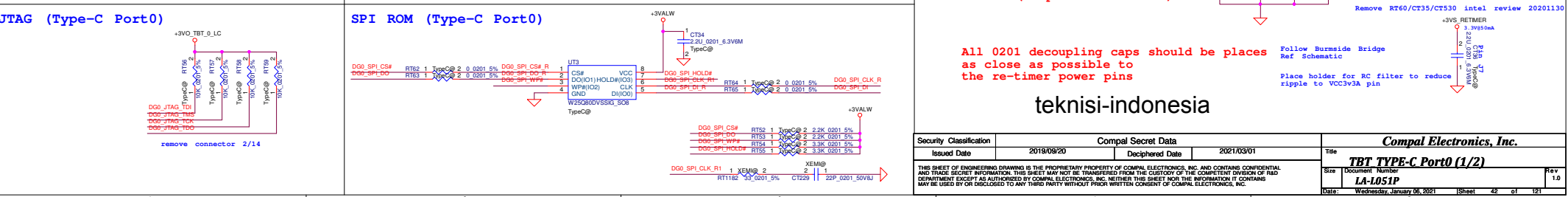
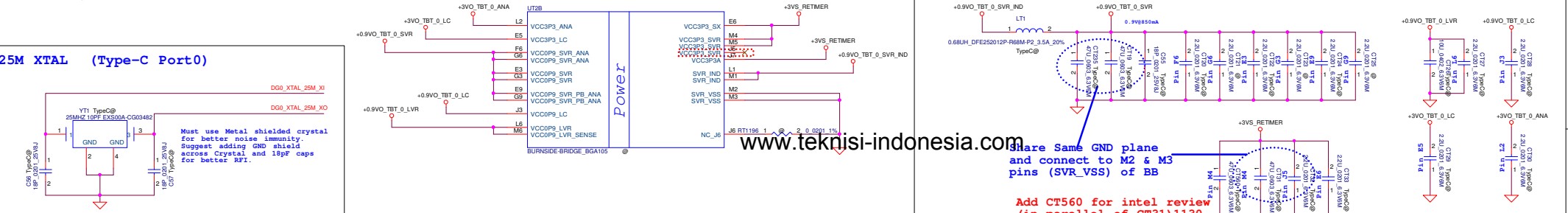
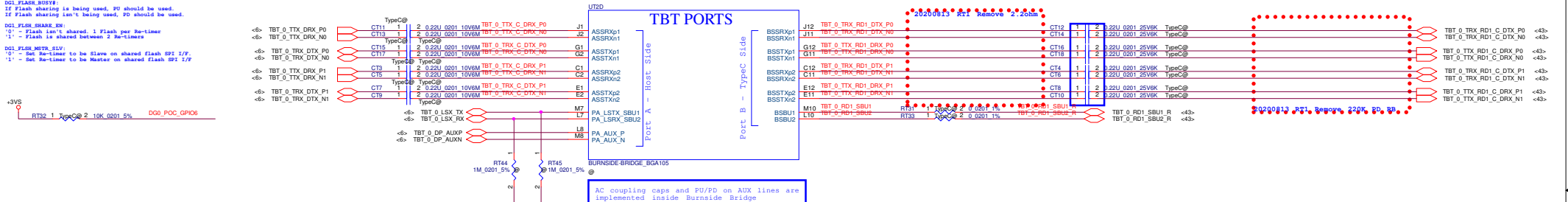
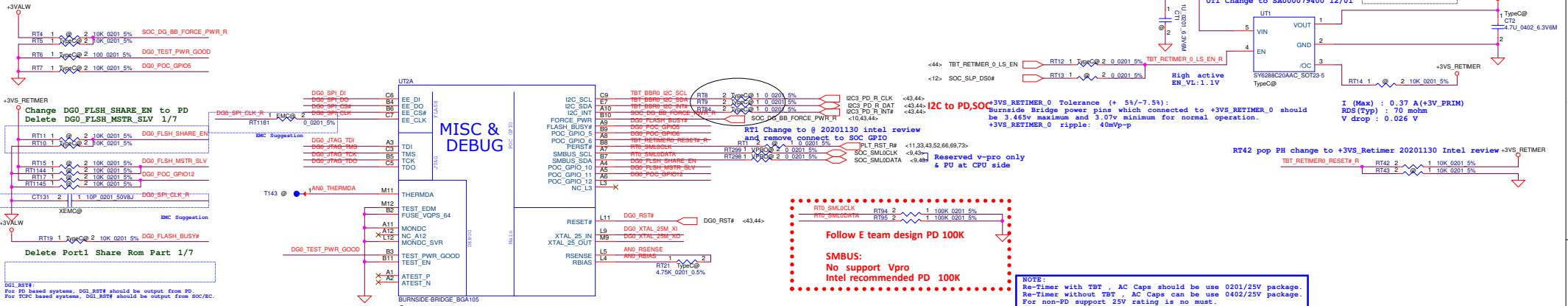


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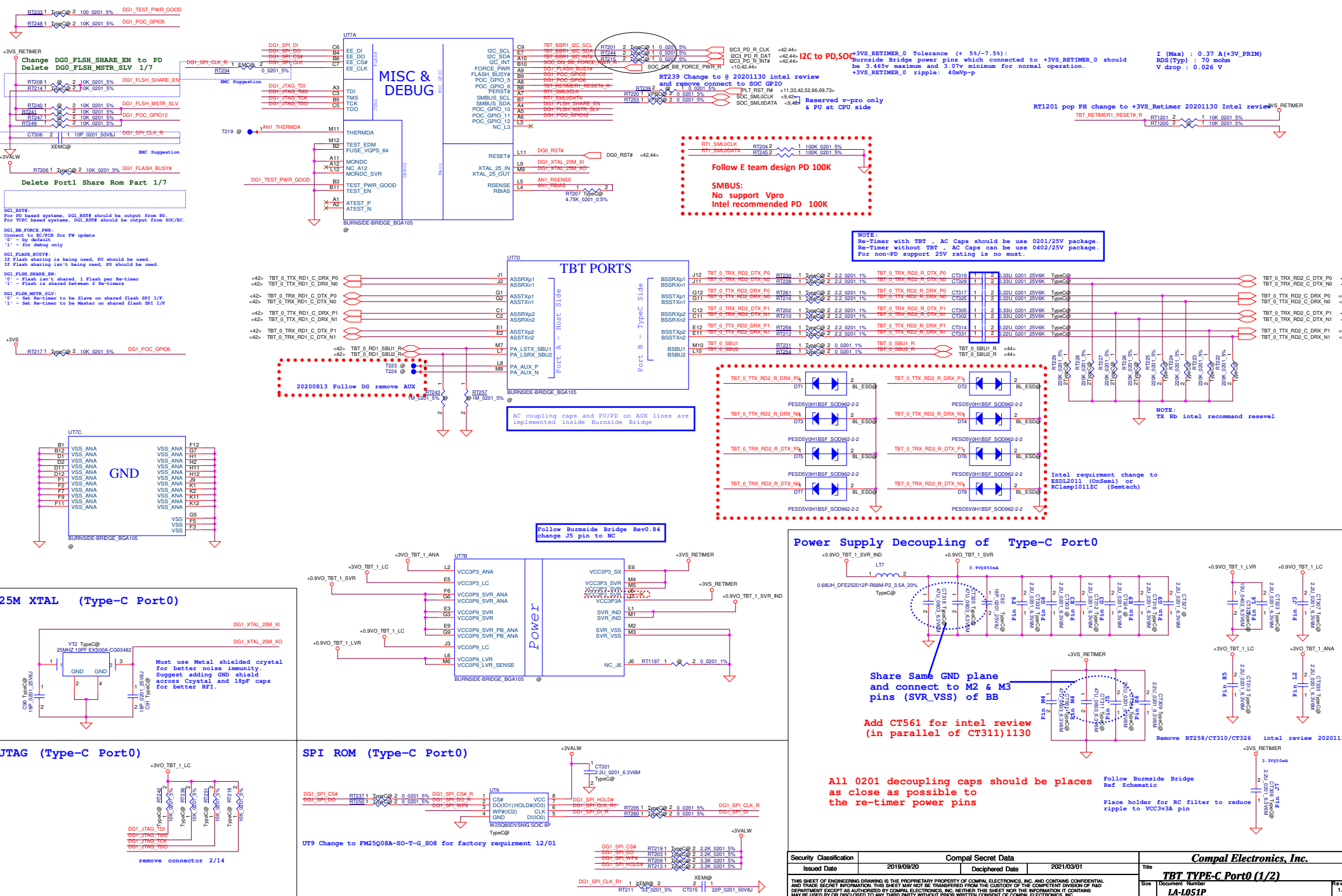
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				Sheet	41 of 121
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## TBT Conn. (Port 0/ Re-Timer1)

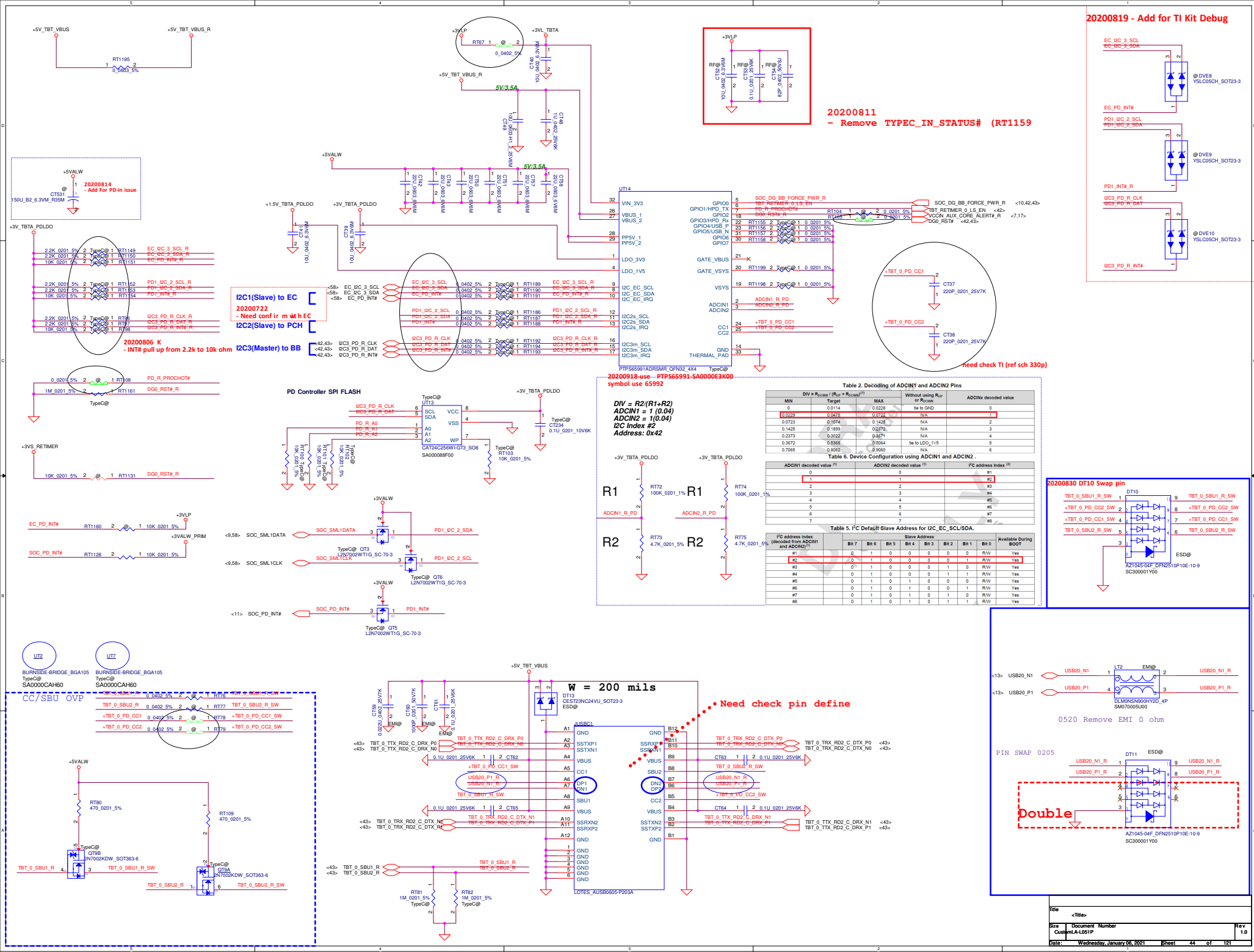


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<b>Date:</b> Wednesday, January 16, 2021			<b>(Sheet) 49 of 121</b>

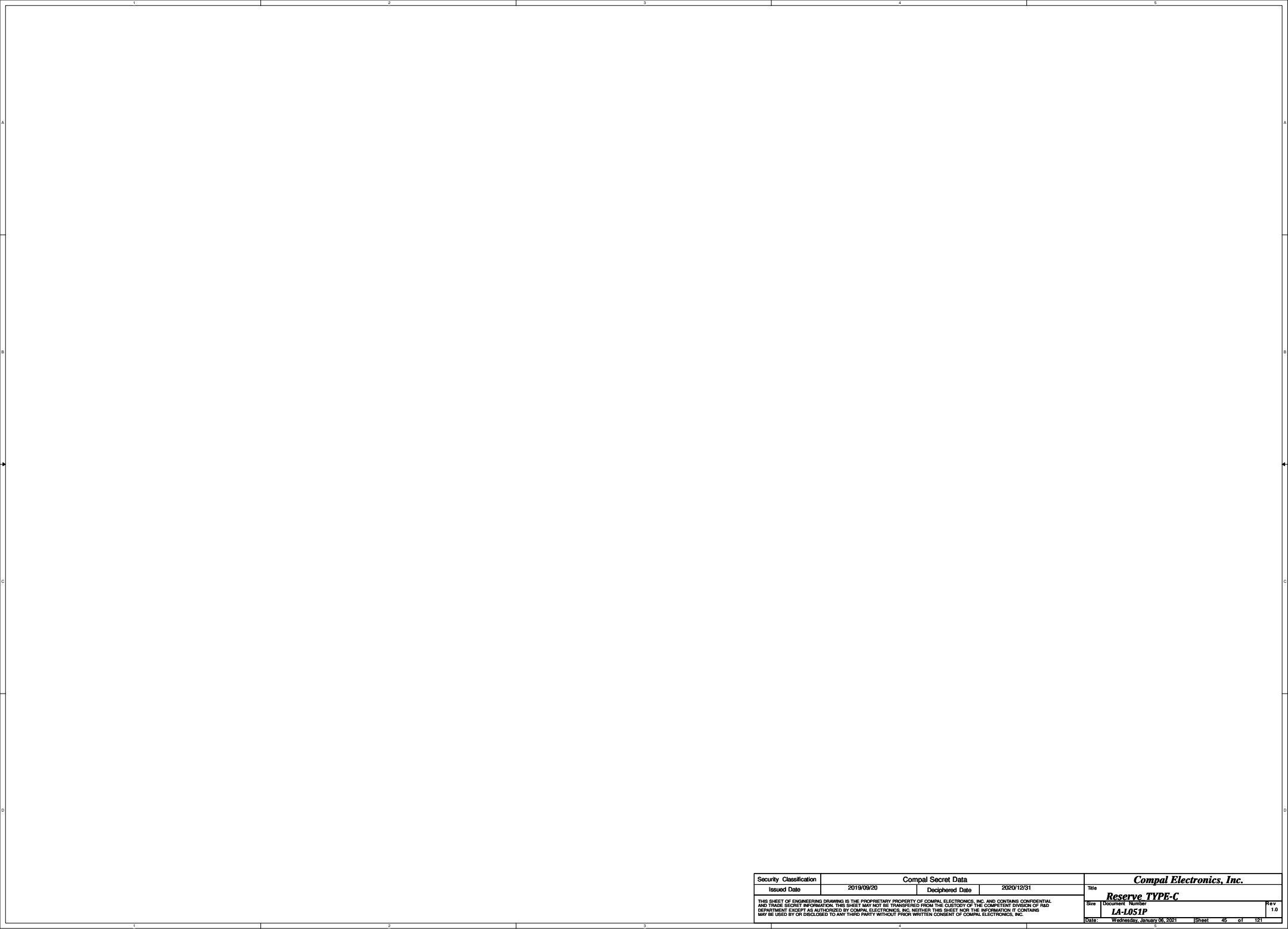
TBT Conn. (Port 0/ Re-Timer2)











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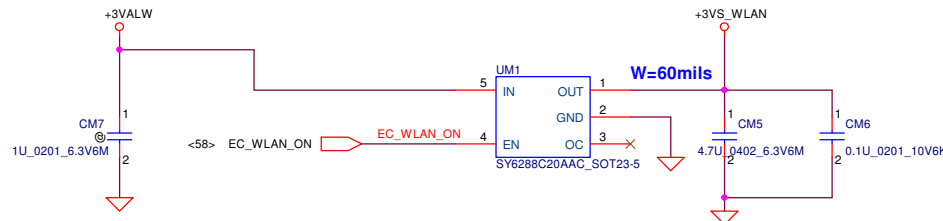
MB\_USB3.1 TypeC Conn. (Power Path)  
- Remove  
- TBT4 Change to TI solution

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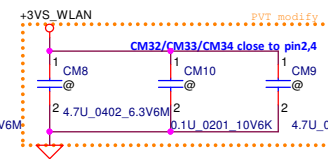
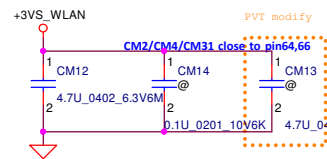
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# NGFF Wireless LAN / BT (Key E) [PCIE+USB/CNVi]



**Remark**  
\* un use EMC (EM5203) for CNVi issue  
\*\* CNVi use ALW power rail / PCIE WLAN use VS rail  
autodetct and change EN pin power domain by BIOS/EC



UART\_EC\_CRXD\_DTXD RM59 1 DEBUG@ 2 0 0402 5% UART\_2\_CRXD\_DTXD  
UART\_EC\_CTXD\_DRXD RM60 1 DEBUG@ 2 0 0402 5% UART\_2\_CTXD\_DRXD

Reserved UART to EC debug connector routing

UART\_2\_CRXD\_R\_DTXD RM2 1 UART@ 2 0 0402 5% UART\_2\_CRXD\_DTXD <12>  
UART\_2\_CTXD\_R\_DRXD RM3 1 UART@ 2 0 0402 5% UART\_2\_CTXD\_DRXD <12>

Co-layout with CNVi for UART Debug and BT signal

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USB2 P10  
(For Bluetooth)

CNVi Rx

PCIE X1

(Link to PiCe Port 12)

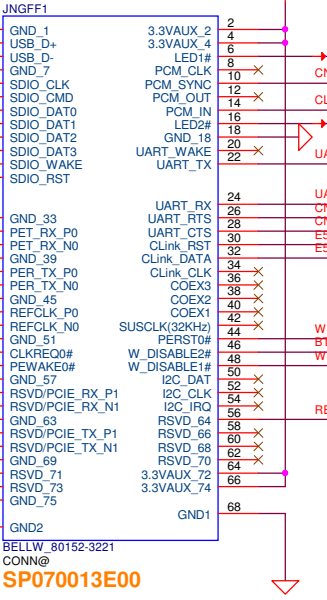
PCIE CLK

(From PCH CLKOUT3)

CNVi Tx

20200828 Swap for Port12 to Port4

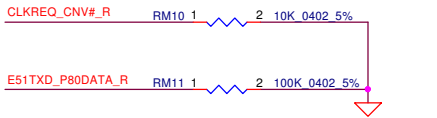
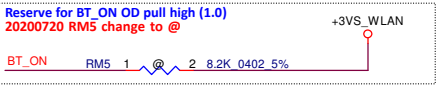
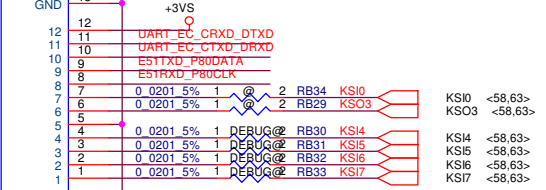
KEY E



SP010028W00

DEBUG@

ACES\_51625-01201-001



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				Rev	1.0



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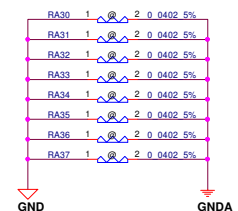
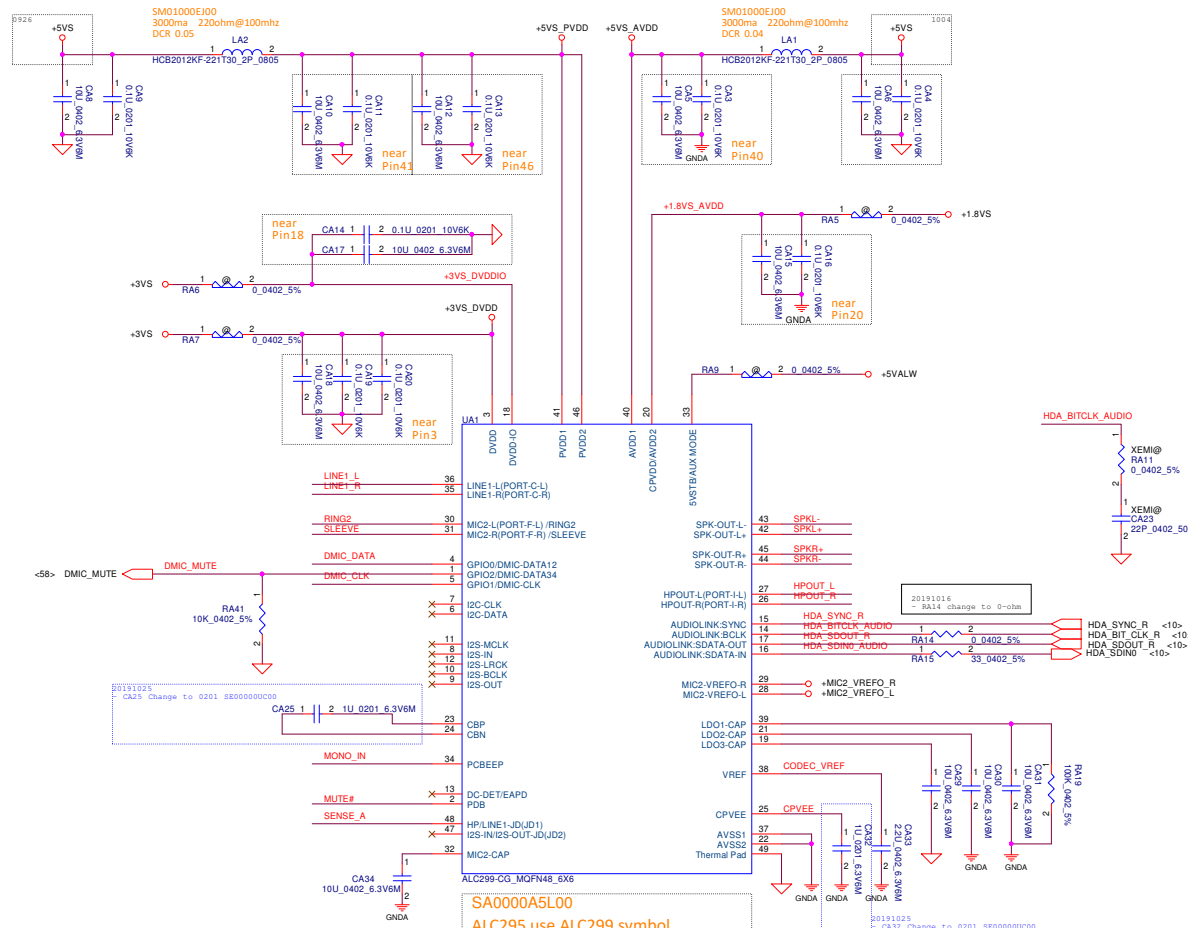
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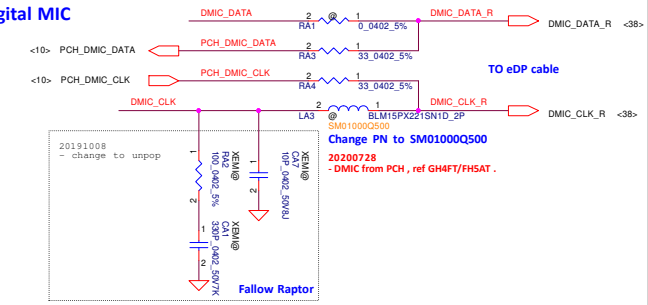
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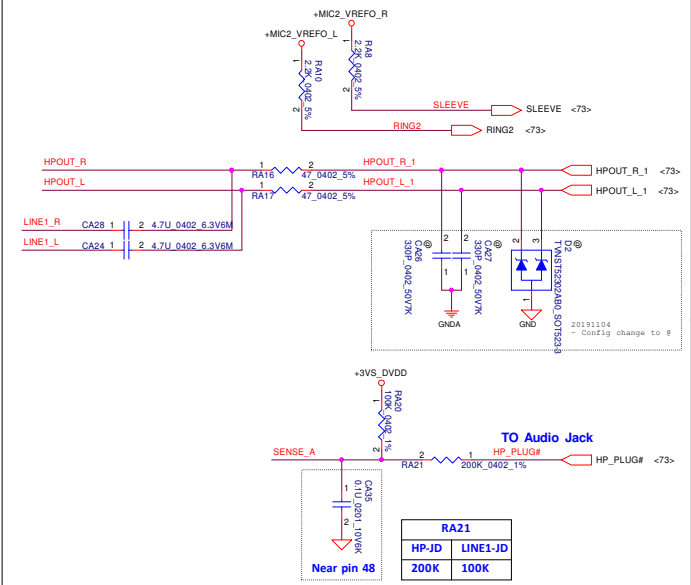
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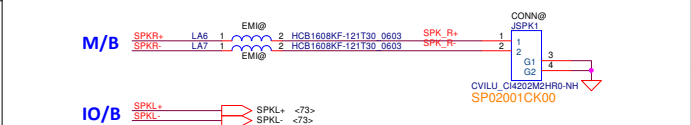
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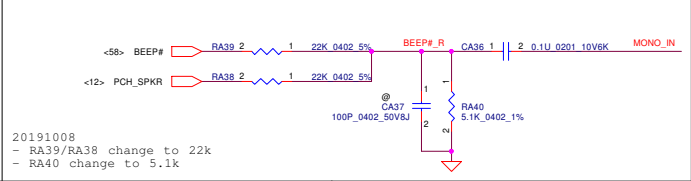
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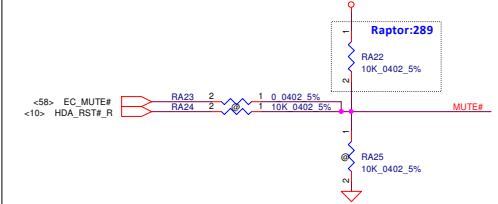
## Speaker



## BEEP



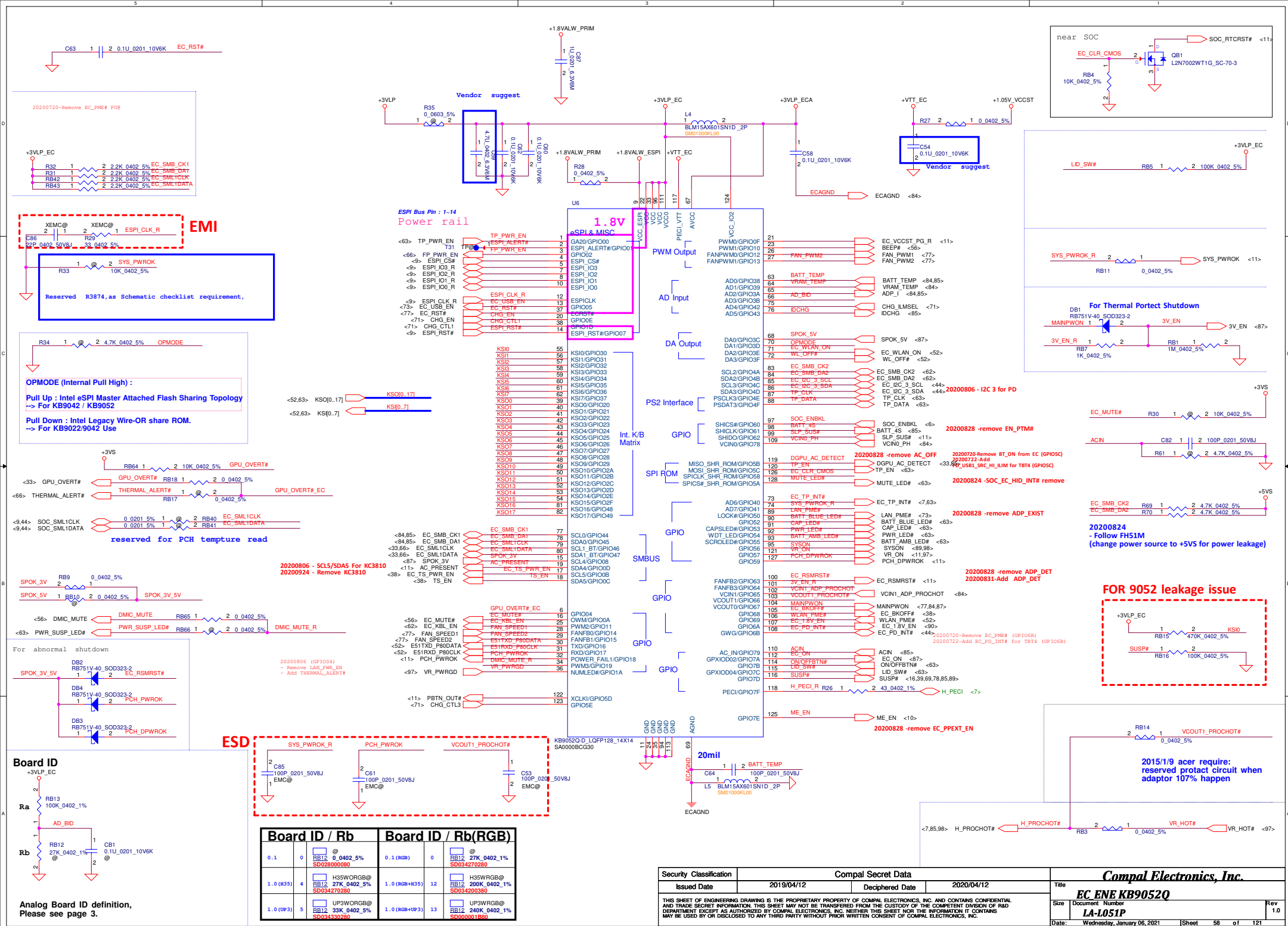
## MUTE#



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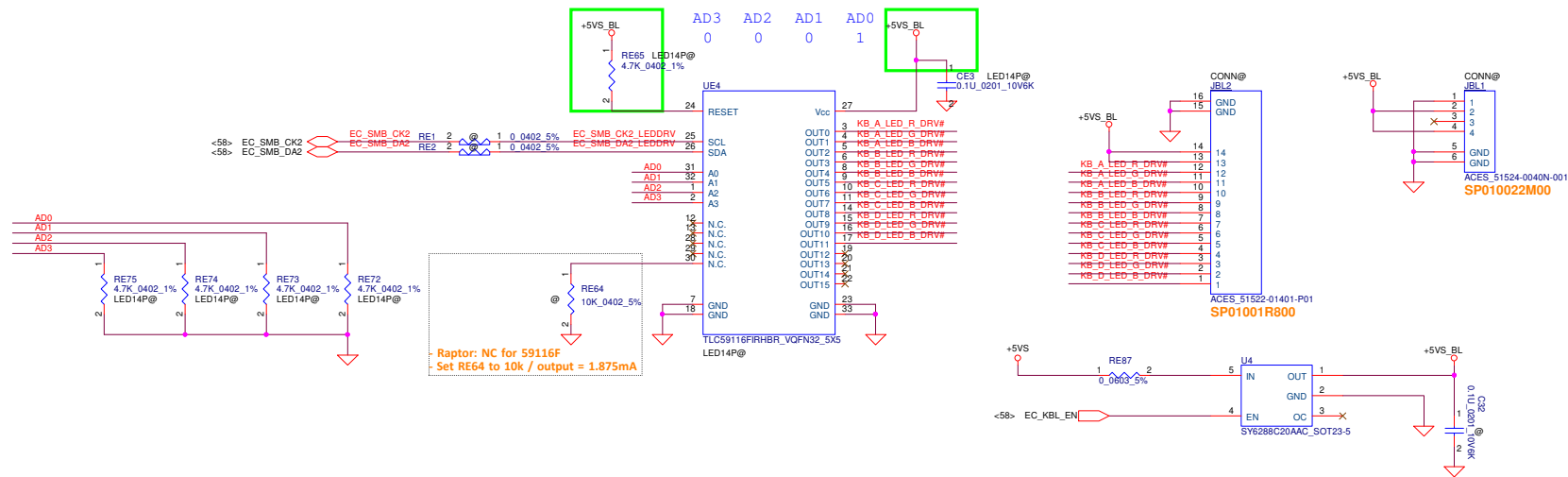


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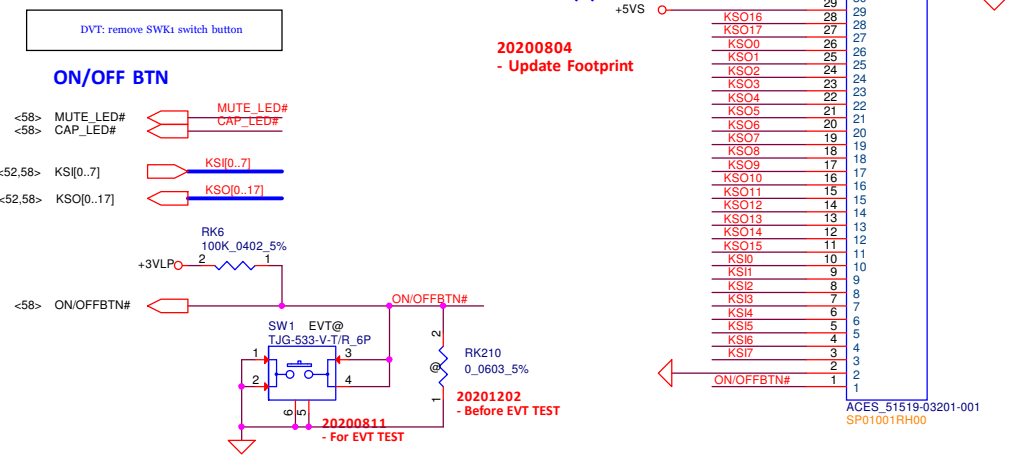
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20200924  
-Remove Pre-Key

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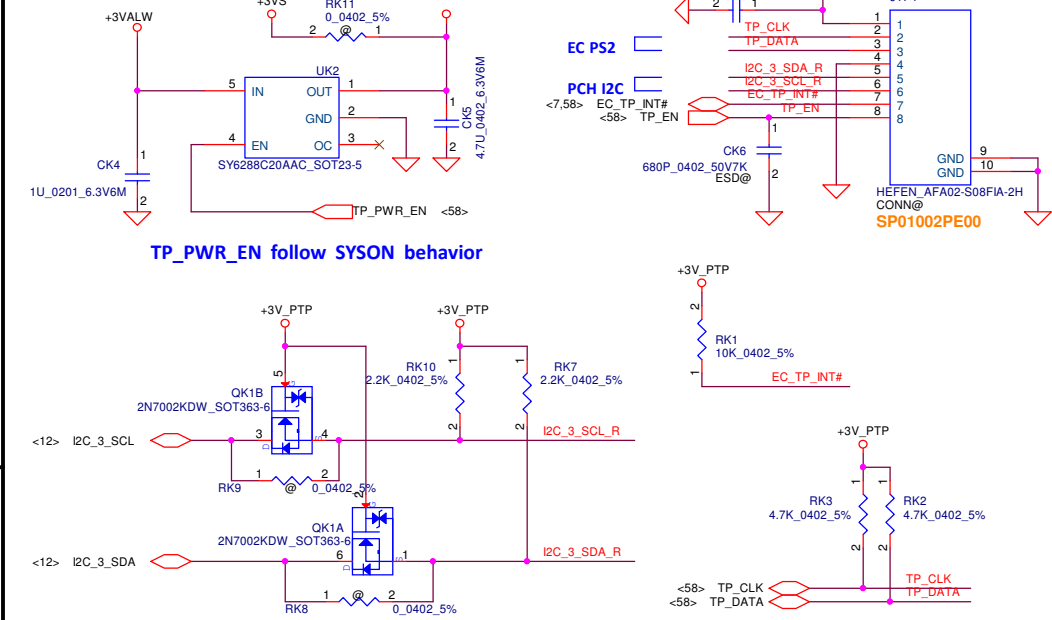
KB Conn. 32pin



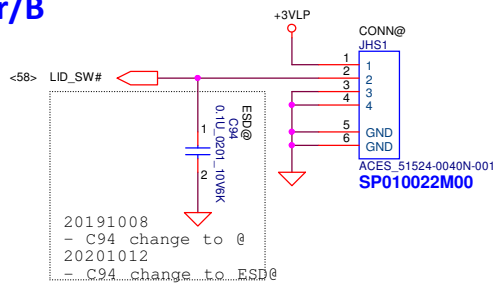
KB BackLight (1 Zone RGB) 6pin

20200823  
- Change to page 62

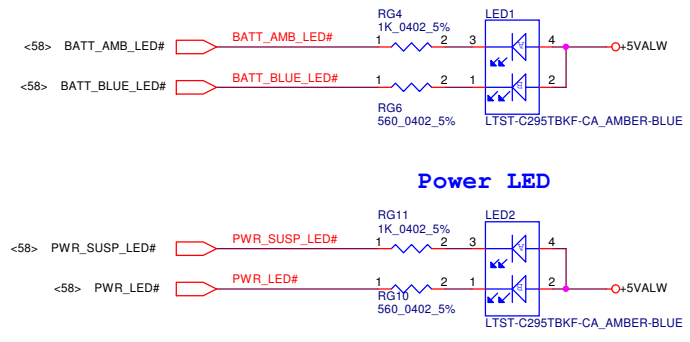
TP/B Conn.



To Hall sensor/B



Battery LED



Turbo Key

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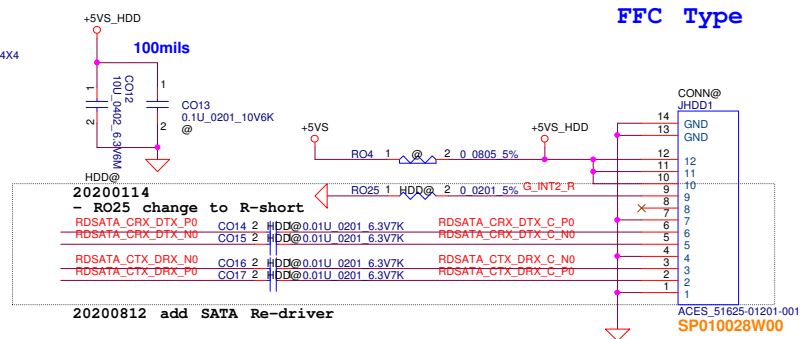
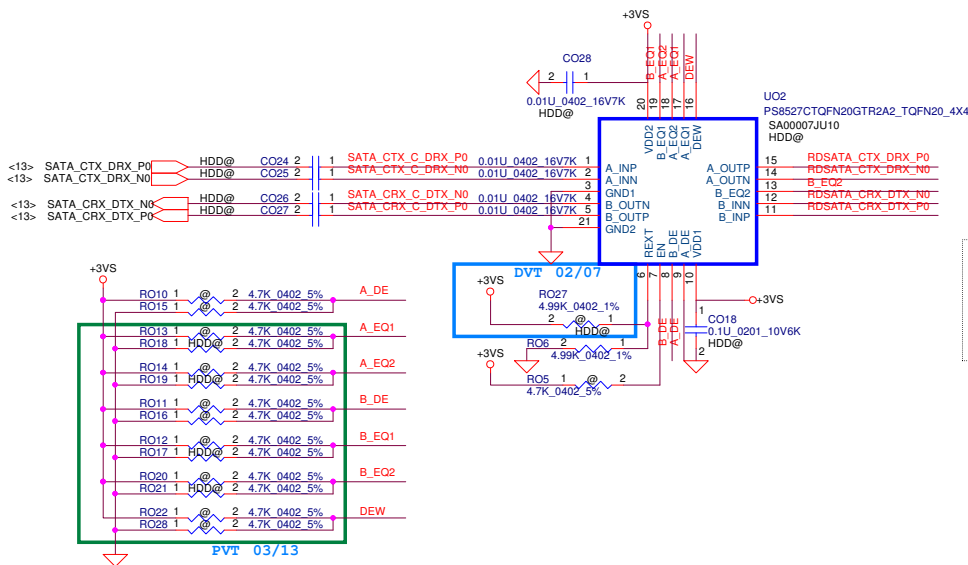
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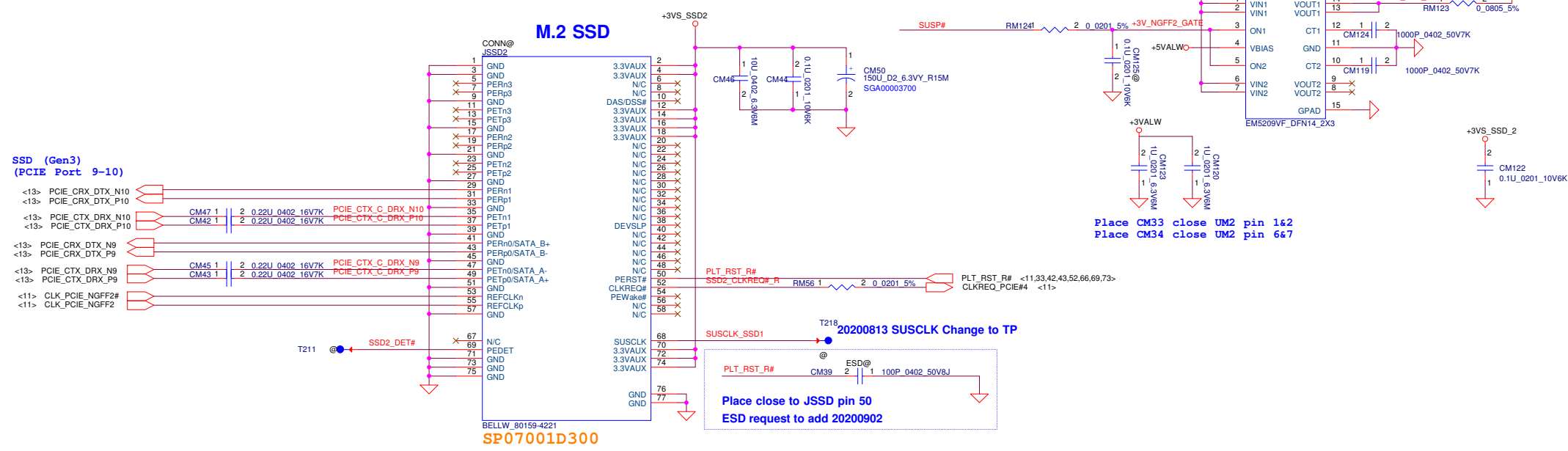
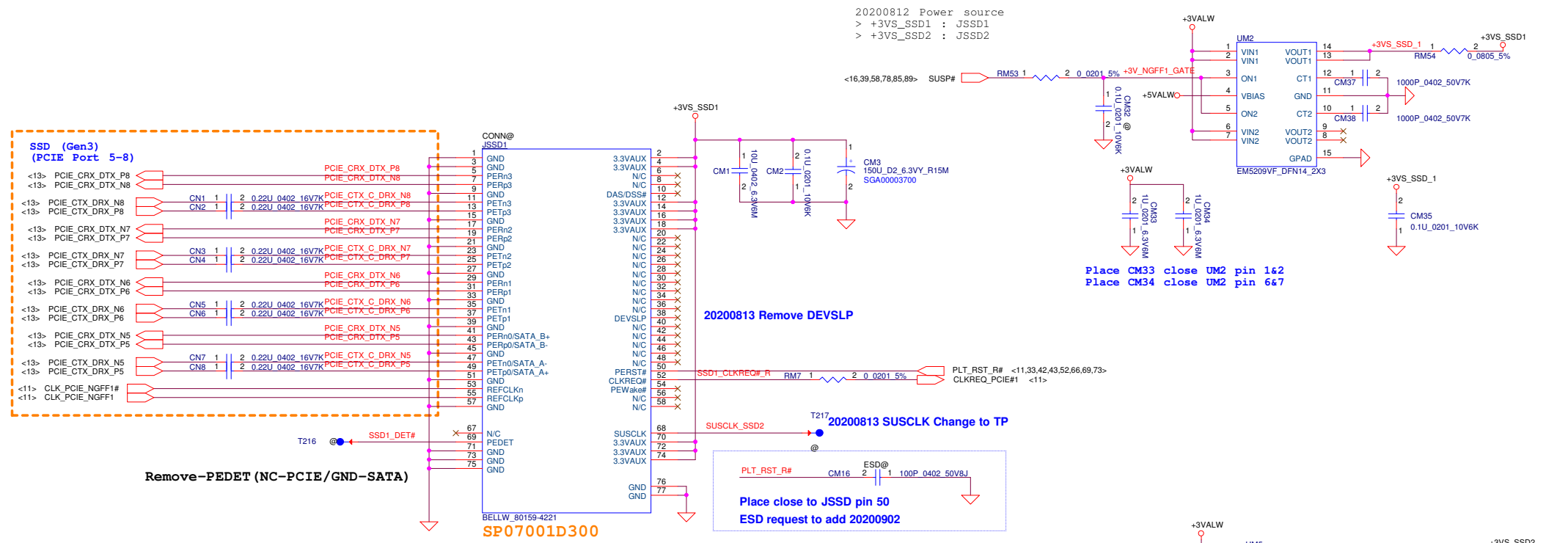


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										LA-L051P	
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20200901 Remove PCIE redrive

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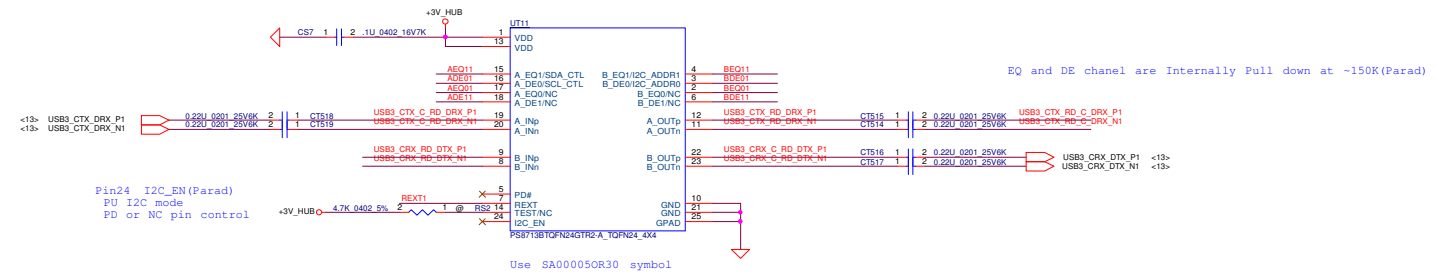
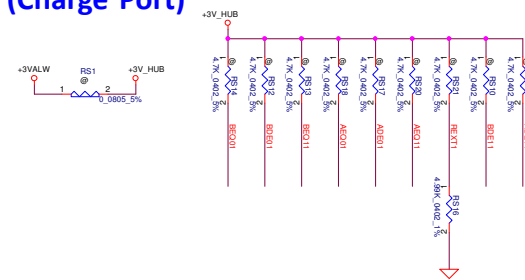


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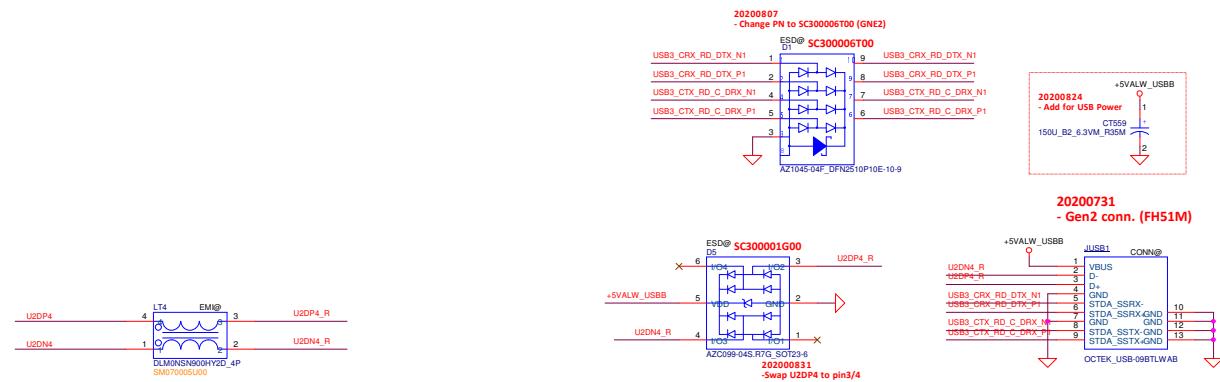
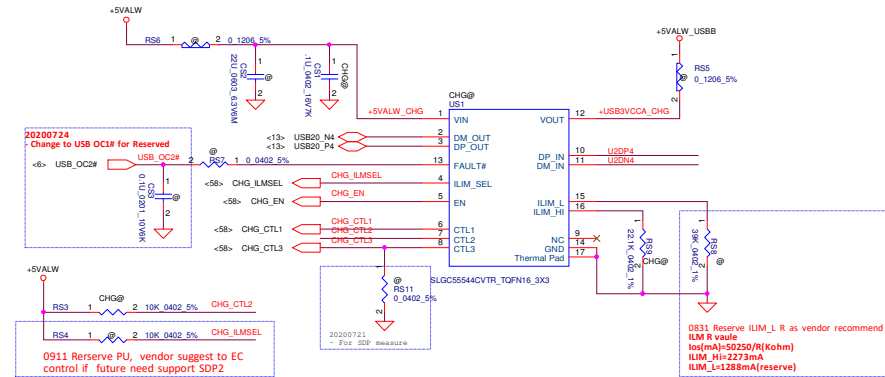
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**MB\_USB3 GEN1(W Re-driver) Type-A Conn.  
(Charge Port)**



## USB Host Charger



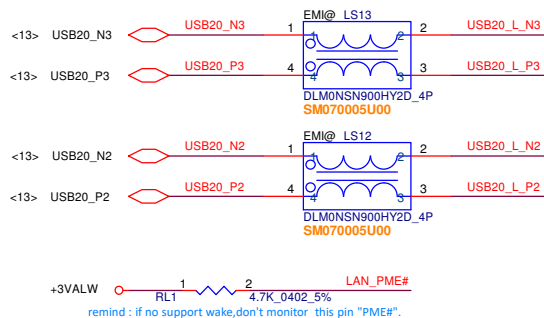
## USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Setting	Limit	Note
0	0	1	0	1	SDP1-OFF	ILIM_H		Port power off
1	0	1	0	1	SDP1	ILIM_H		Data Lines Connected
1	0	1	1	1	DCP Auto	ILIM_H		Data Lines Disconnected
1	1	1	1	1	CDP	ILIM_H		Data Lines Connected

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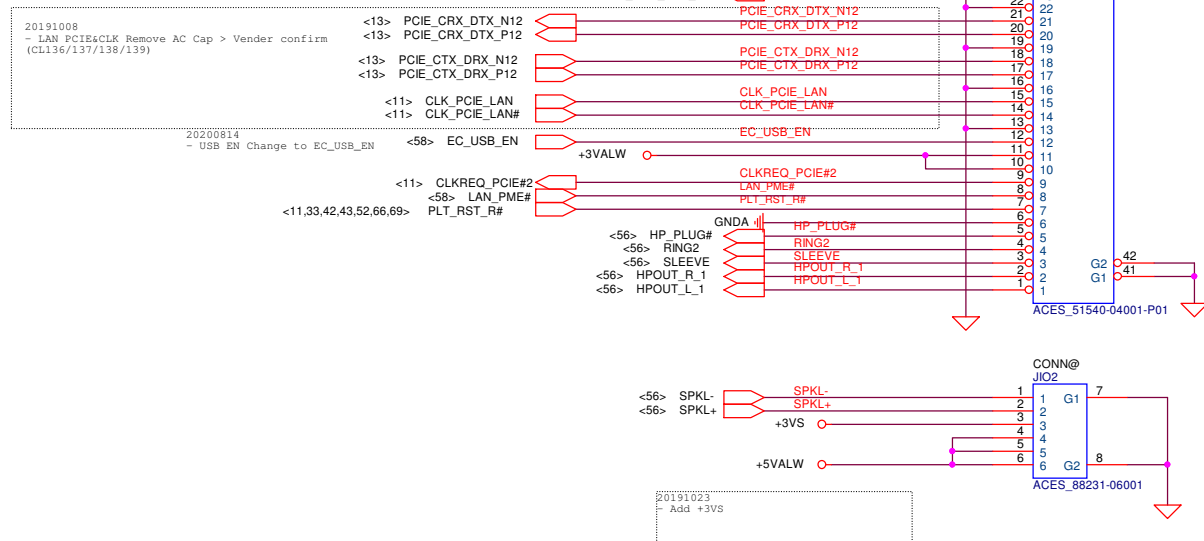
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## IO/B CONN



```
1209A
- IO_B change pin define
```

20200828 Swap for Port4 to Port12



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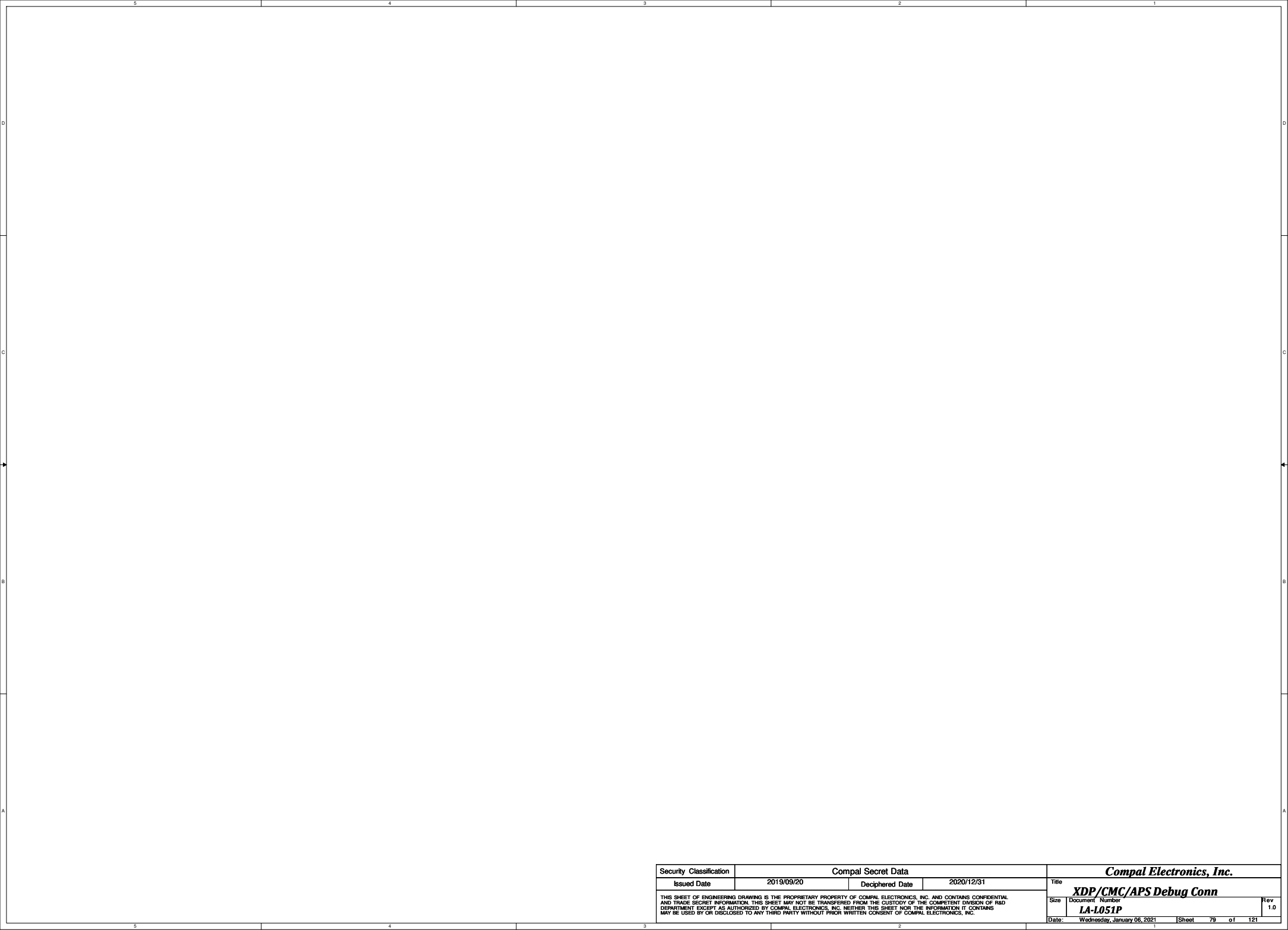
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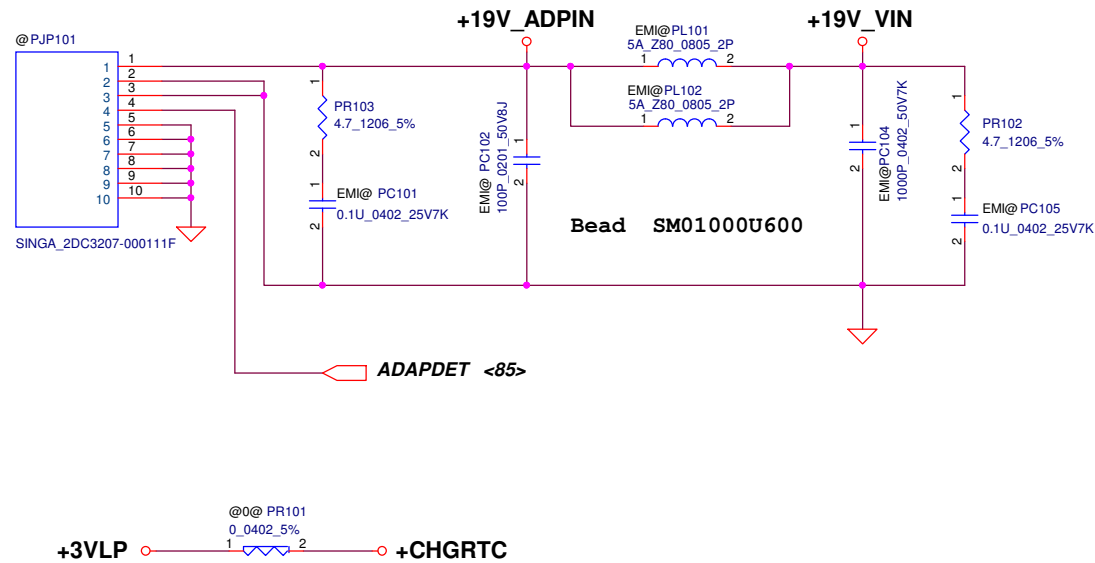
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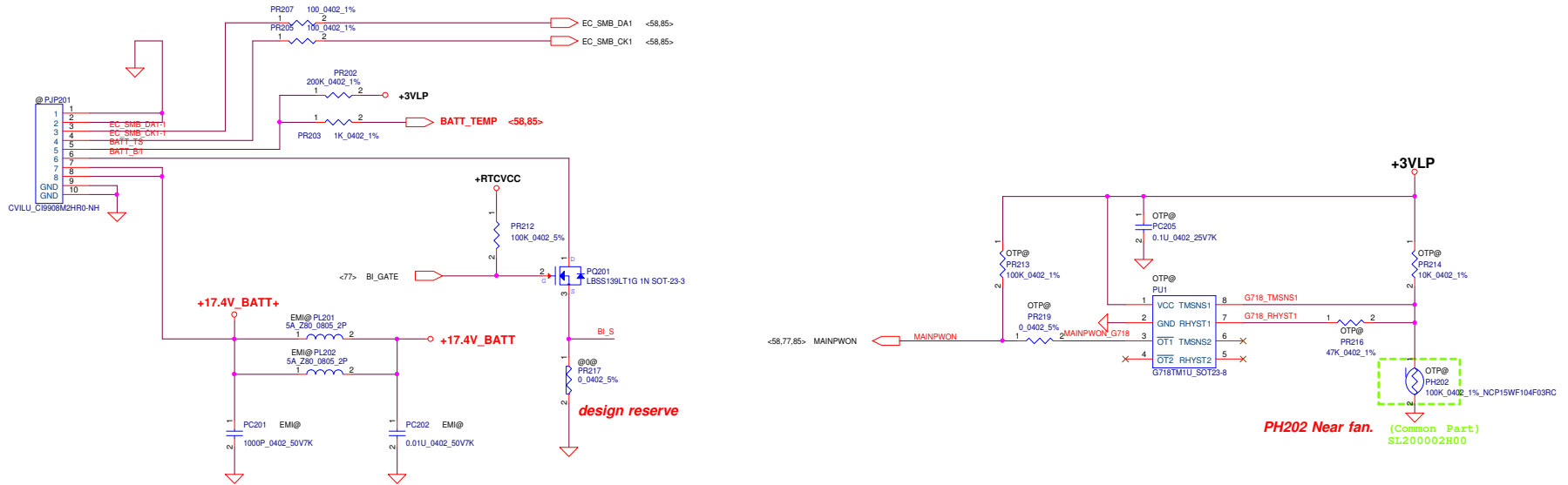
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# Battery Bot Side

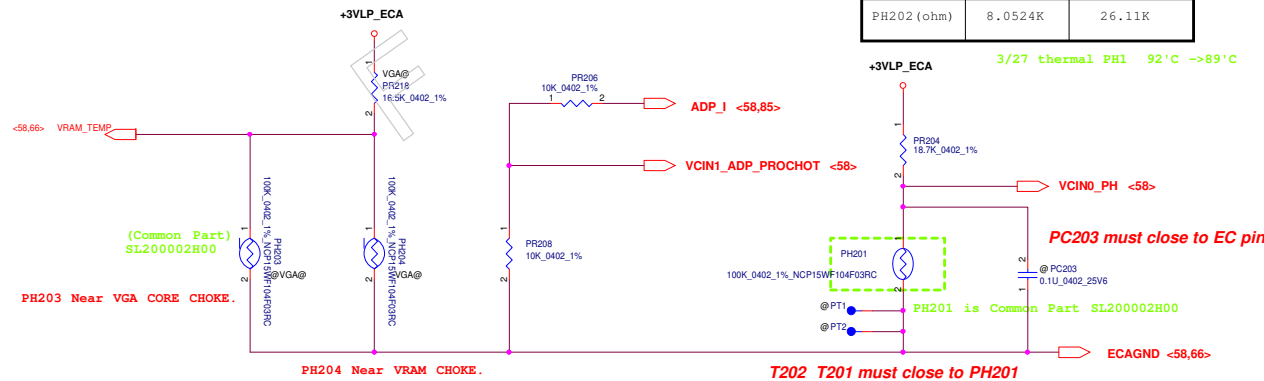
PIN1 GND  
PIN2 GND  
PIN3 SMD  
PIN4 SMC  
PIN5 TEMP  
PIN6 BI  
PIN7 Batt+  
PIN8 Batt+



When PR204=18.7K

For KB9022 OTP	Active	Recovery
VCIN0_PH (V)	89°C, 1V	56°C, 2V
PH202 (ohm)	8.0524K	26.11K

3/27 thermal PH1 92°C -> 89°C

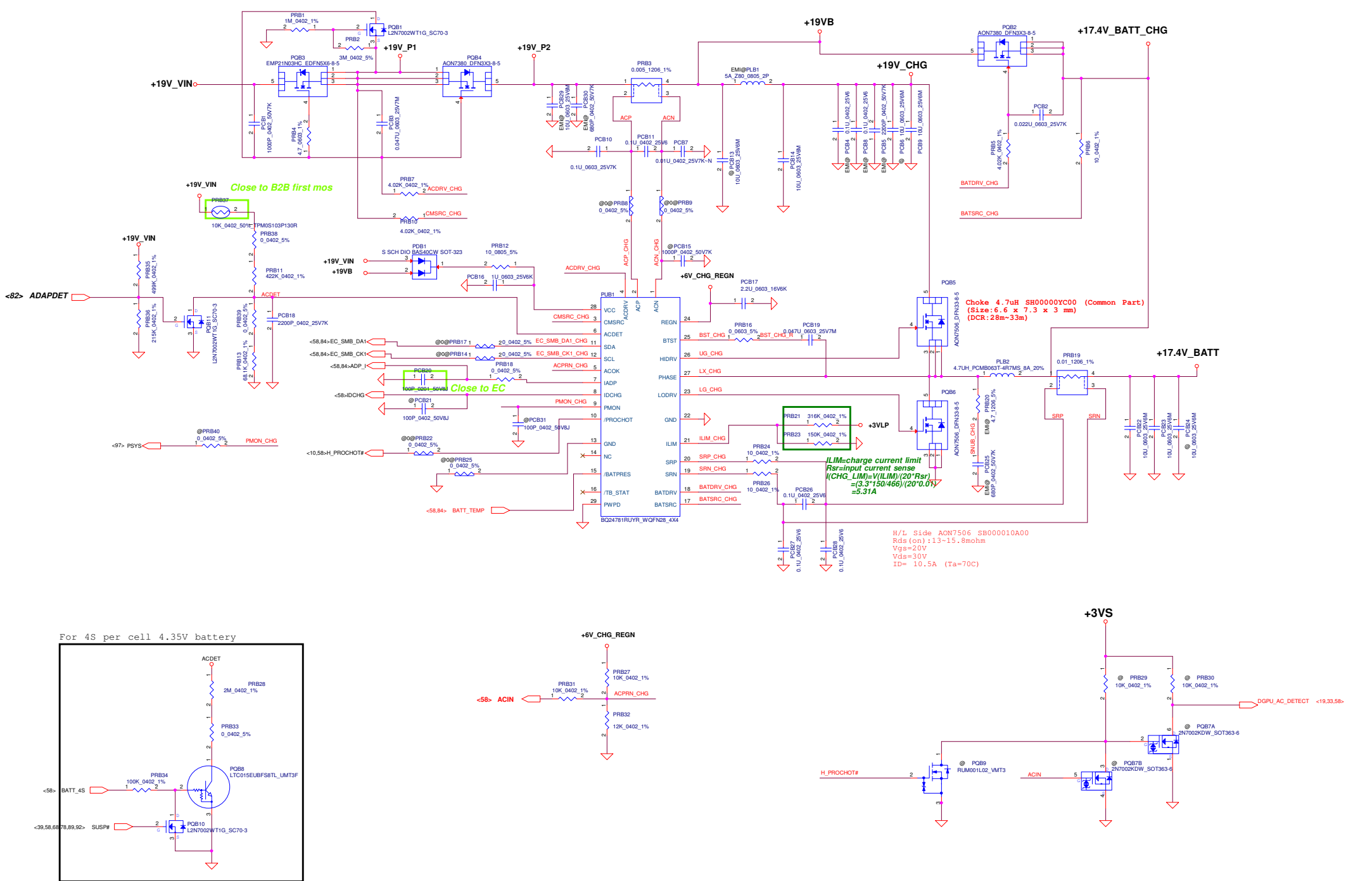


$$ADP\_I = 20 * I(\text{adapter}) * 0.01$$

$$I(\text{adapter}) = \text{adapter}(W) * 130 / 19$$

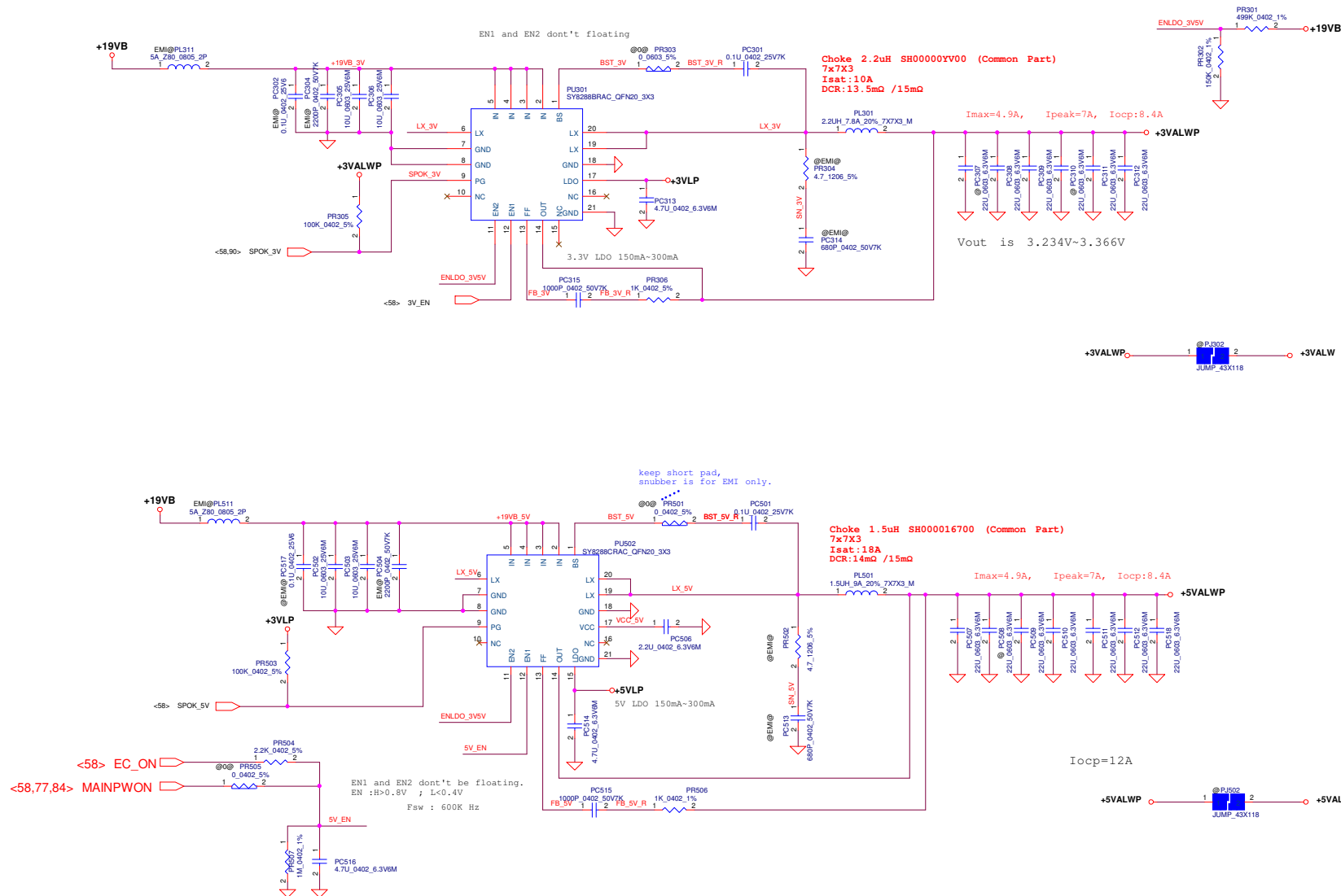
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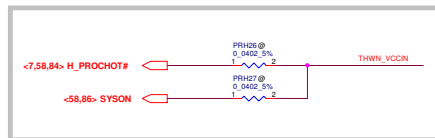
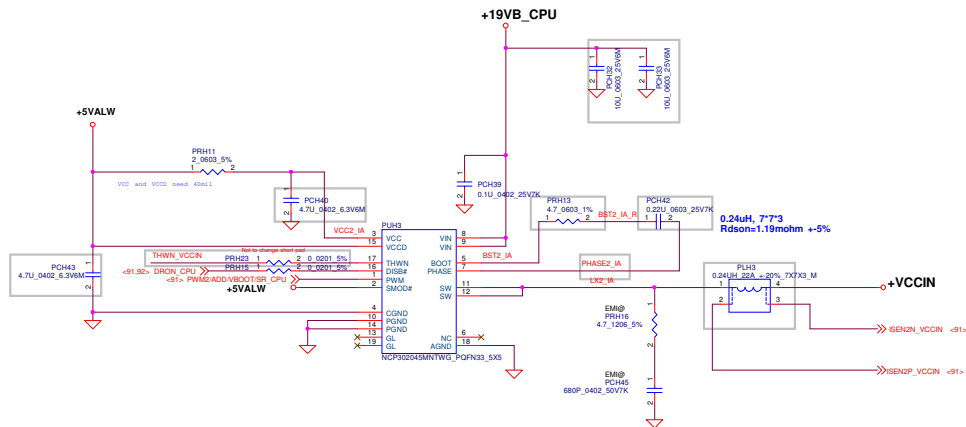
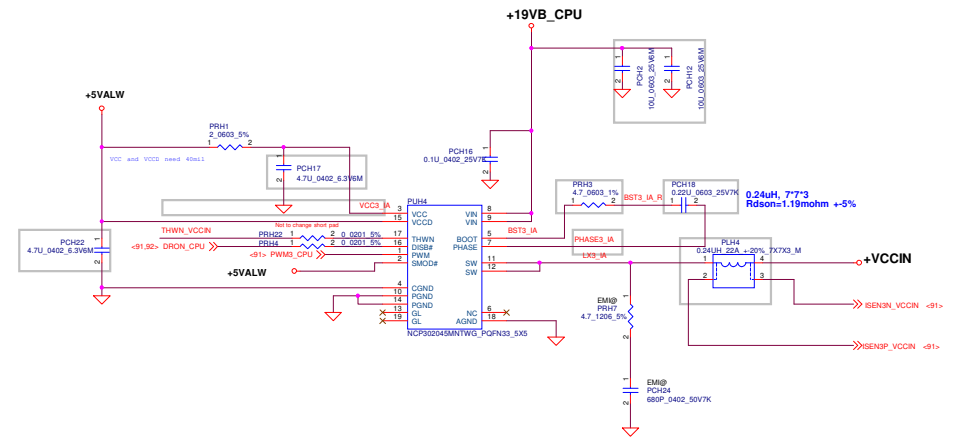
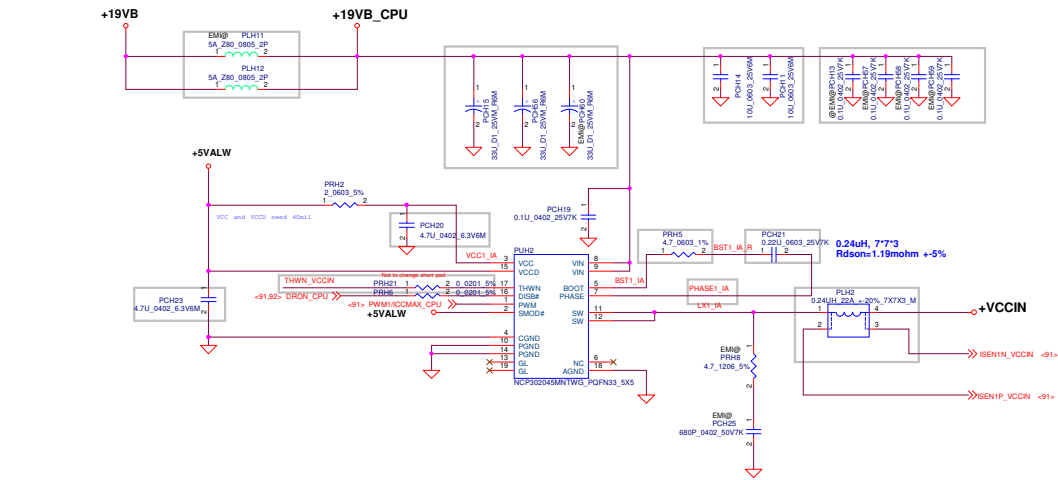
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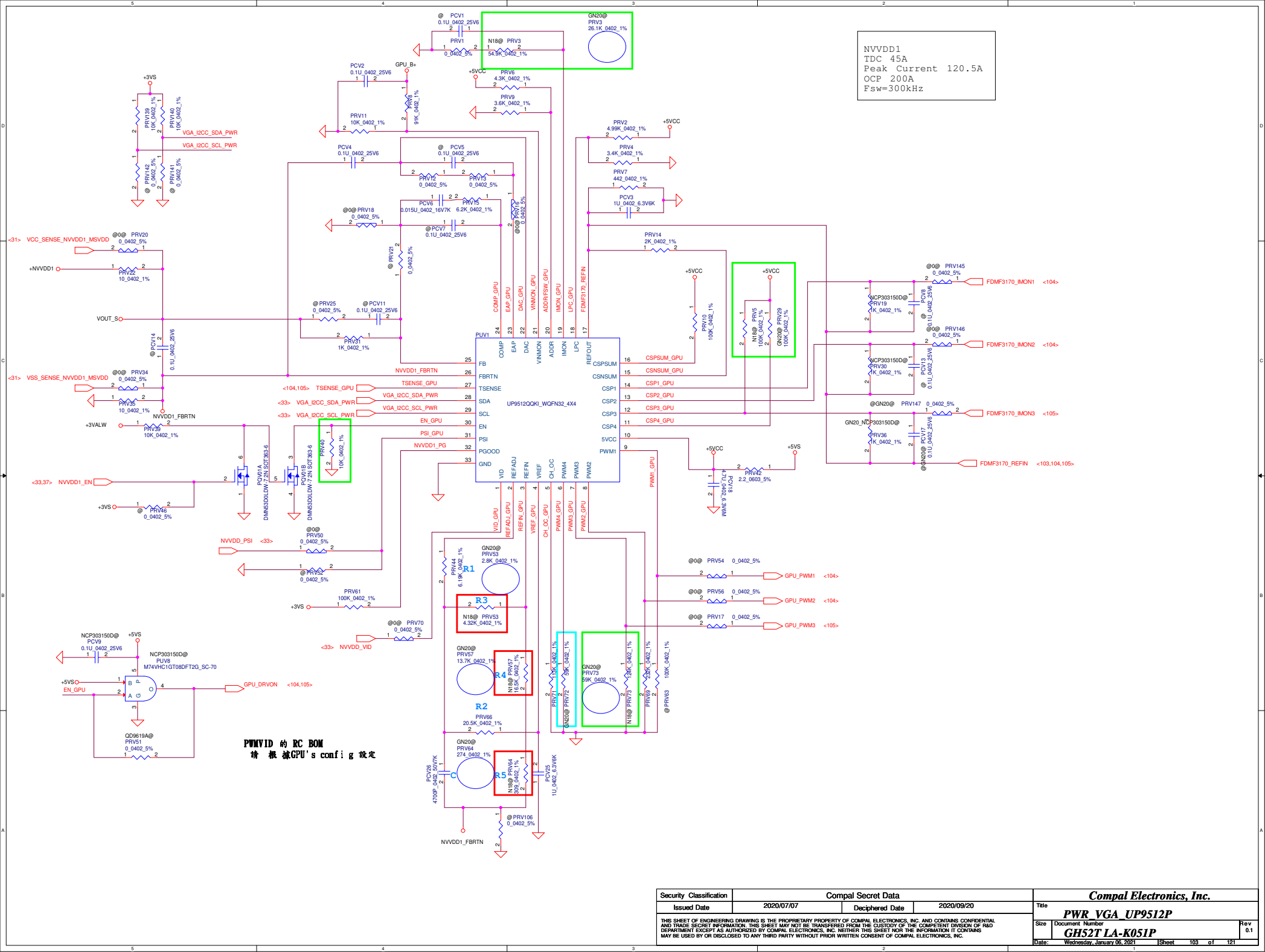
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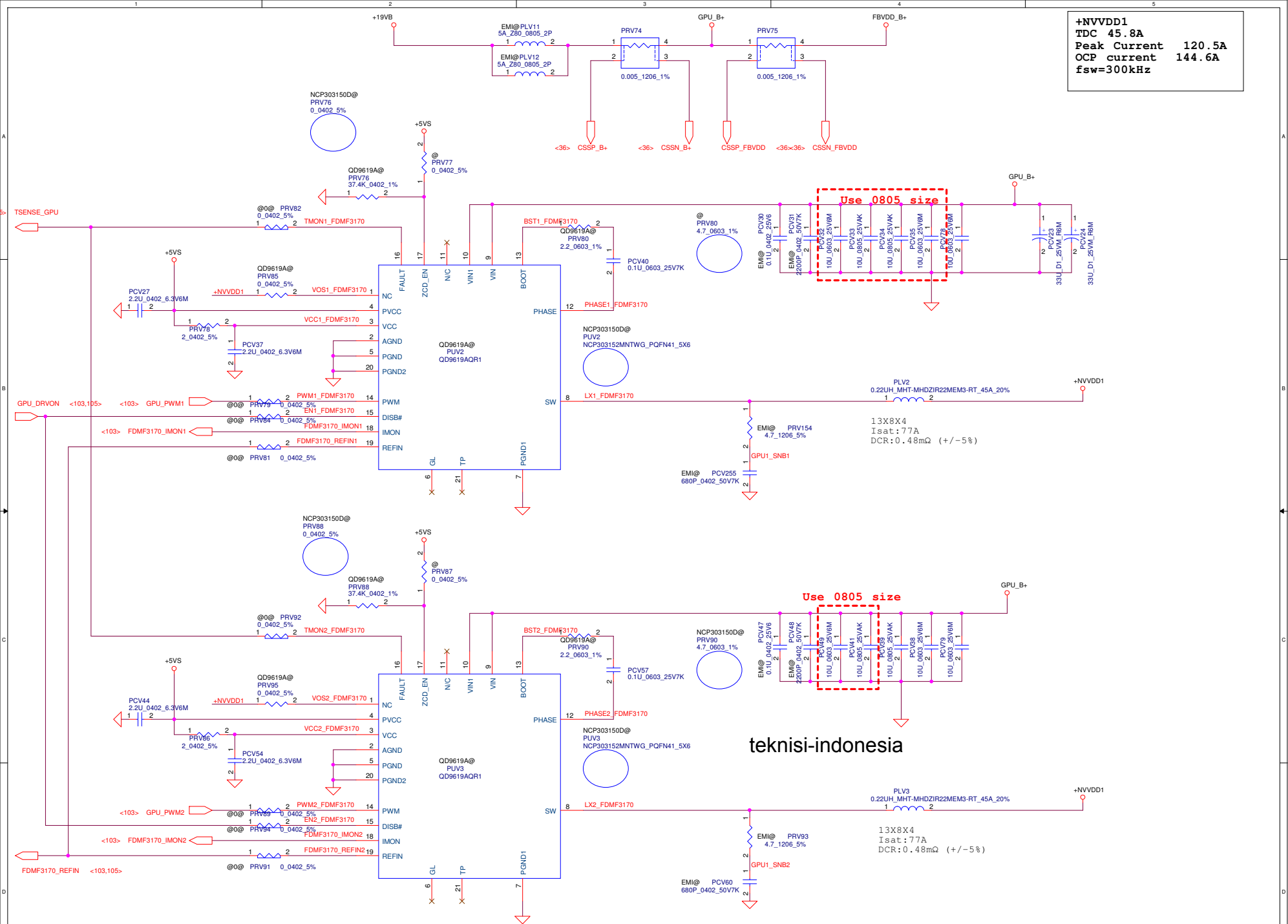


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**+NVVDD1**  
**TDC 45.8A**  
**Peak Current 120.5A**  
**OCF current 144.6A**  
**fsw=300kHz**



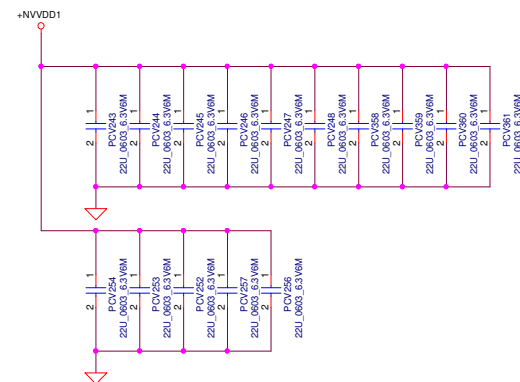
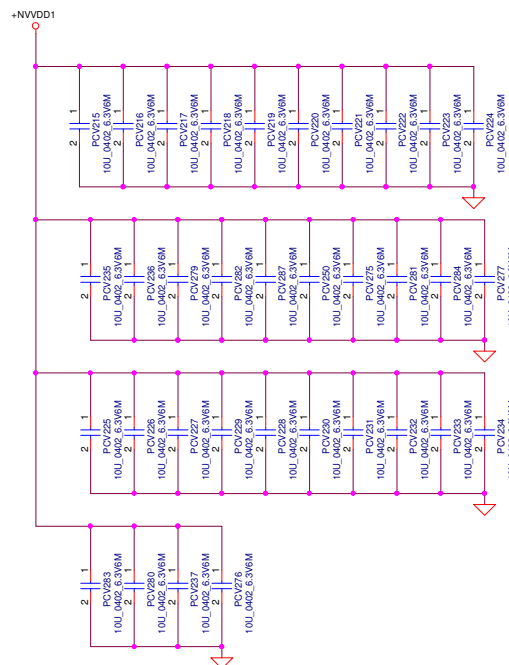
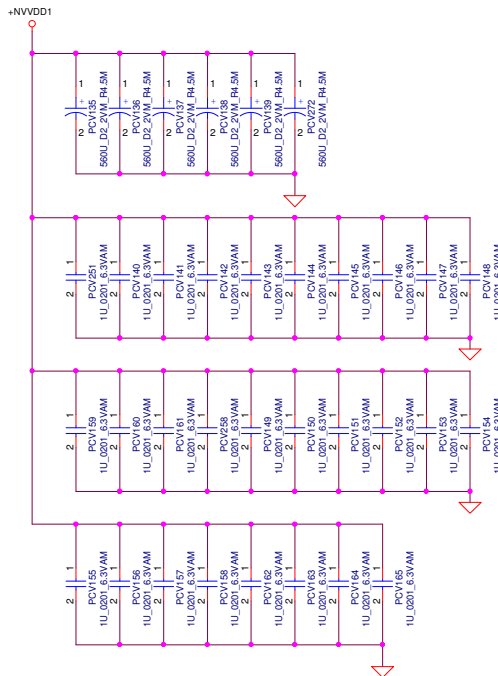
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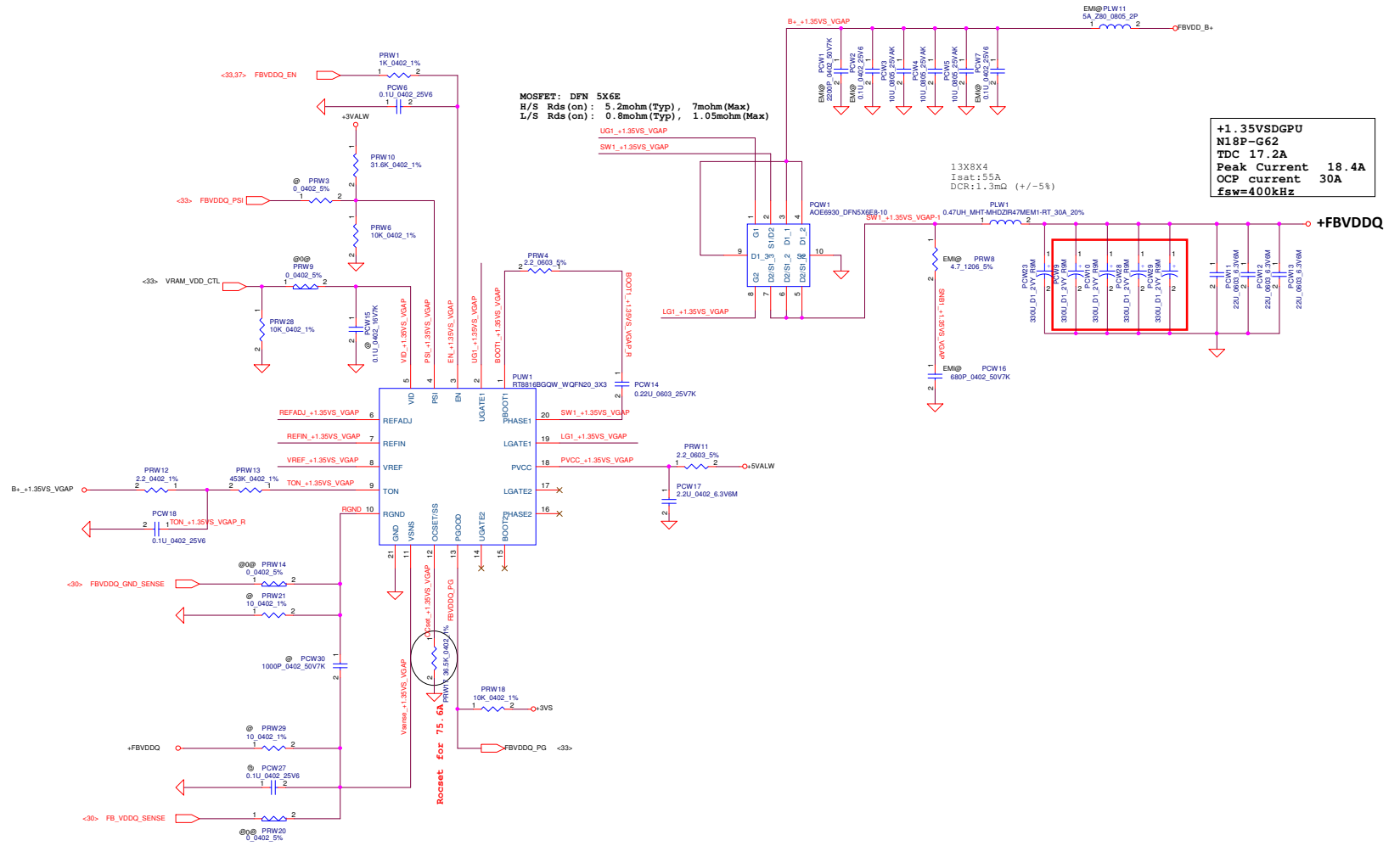
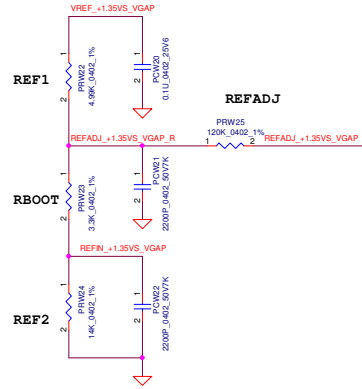
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+NVVDD  
560uF X 6  
22uF\_0603 X 15  
10uF\_0402X 34  
1uF\_0201 X 28



Samsung & Micron VRAM  
When, VRAM\_VDD\_CTL=High  
Vboot=1.25V  
When, VRAM\_VDD\_CTL=Low  
Vboot=1.2V



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PWR

Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
01	NA	for cost down		PUZ1 change from ncp81215m_SA0000AQE00 to ncp81215p_SA0000CTW00 PCZ24, PCZ27 change from 82P_0402_SE000014700 to 82p_0402_SE071820J80 PCB17 change from 2.2u_0603_25V_SE00000WP00 to 2.2u_0603_16V_SE000006S80 PCB20 & PCB21 change from 100p_0603_SE024101J80 to 100p_0402_SE071101J80 PCM6 change from 10u_0603_SE000005T80 to 22u_0603_SE00000M000 PCM7 10u_0603_SE000005T80 change to unpop PRB12 change form 10_1206_SD011100A80 to 10_0805_SD002100A80	1202	DVT
02	NA	avoid incomplete replacement	P85	PQB1 & PQB11 change from 2n7002_SB000009Q80 to 2n7002_SB00001GE00	1202	DVT
03	NA	sourcer request	P84	PQ201 change from BSS139_SB00001GD00 to BSS138_SB00000PF00	1202	DVT
04	NA	NA	P85	Add PRB37 & PRB38 & PRB39 0_0402_SD028000080. avoid chager B2B damage	1209	DVT
05	NA	for acoustic noise	P97	Co-lay PCV362~PCV369 10u_0603_SE00000X210 for acoustic noise.	1209	DVT
06	NA	for acoustic noise	P100	Co-lay PCW24~PCW26 10u_0603_SE00000X210 for acoustic noise.	1209	DVT
07	NA	CPU transient	P91	PRZ49 change from 274k_0402_SD034274380 to 165k_0402_SD034165380 PRZ14 change from 28k_0402_SD034280280 to 29.4k_0402_SD034294280	1212	DVT
08	NA	CPU transient	P95	PCZ101 330u_D2_SGA00009S00 change to unpop for CFL PCZ102 & PCZ103 330u_D2_SGA00009S00 change to SMT for CFL PCZ108, PCZ109, PCZ110, PCZ112, PCZ119, PCZ125, PCZ133, PCZ137 change to SMT for CFL PCZ163, PCZ164, PCZ165, PCZ166, PCZ167, PCZ168 1u_0201_SE00000UC00 change to SMT for CFL PCZ107, PCZ113, PCZ114, PCZ115, PCZ116, PCZ121, PCZ123, PCZ127, PCZ128, PCZ130, PCZ131, PCZ132, PCZ172, PCZ173, PCZ174 change to unpop for CFL PCZ104, PCZ105, PCZ107, PCZ111, PCZ113, PCZ114, PCZ115, PCZ116, PCZ118, PCZ120, PCZ121, PCZ123, PCZ124, PCZ126, PCZ127, PCZ128, PCZ130, PCZ131, PCZ132, PCZ134, PCZ135, PCZ136, PCZ138, PCZ172, PCZ173, PCZ174 22u_0603_SE00000M000 change to unpop for CML	1212	DVT
09	NA	for efficiency	P100	PRW13 change from 383k_SD034383380 to 453k_SD034453380	1212	DVT
10	NA	for DFB issue	P85	PRB3 footprint change from R_1206_4P to R_1206_4P-D	0114	PVT
11	NA	NA	P100	reserve PCW28 & PCW29 330_D1_SGA00009S00	0114	PVT
12	NA	NA	P84	PH204 SL200002H00 change to SMT PH203 SL200002H00 change to unpop	0114	PVT
13	NA	NA		PR217, PRB22, PRB25, PRV50, PRV51, PRW9 change from 0_0402 to R-short	0114	PVT
14	NA	for DFB issue	P85	PRB19 footprint change from R_1206_4P to R_1206_4P-D	0116	PVT
15	NA	NA	P95	PCZ138 & PCZ174 change to SMT for CML	0122	PVT
16	NA	HW request	P90	PRH5 change from 12k_0402_SD034120280 to 12.4k_0402_SD00000AJ80	0122	PVT
17	NA	cost down	P90	PCB1 change from 1000P_0603_SE025102K80 to 1000P_0402_SE074102K80	0225	Pre-MP
18	NA	cost down		PC101, PC105, PC301, PC501, PC1102, PC1106, PC1810, PCH4, PCZ58, PCZ59, PCZ60 change from 0.1u_0603_SE042104K80 to 0.1u_0402_SE00000W210	0225	Pre-MP
19	NA	EMI request	P85	add PCB29 10u_0603_SE00000X200 add PCB30 680p_0402_SE074681K80	0225	Pre-MP
20	NA	ESD request	P88	PRM5 change from 6.19k_SD034619180 to 6.34k_SD034634180	0225	Pre-MP
21	NA	avoid B2B mos burn	P85	PRB37 change from 0_0402_SD028000080 to therm_10k_SL200003200 PRB13 change from 66.5k_SD034665280 to 68.1k_SD034681280	0312	Pre-MP
22	NA	QD9619 shortage	P96 P97	PRV51 change from R_short to 0_0402_SD028000080 PRV85 & PRV95 change from R_short to 0_0402_SD028000080		

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Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
01	Design Update	For EA Turning and HW sequence	93, 94 95, 97 89, 92	change PR1009 from 100K_0402_5% (SD028100380) to 10K_0402_5% (SD028100280) change PG pull high from +3VS to +3VALW change PRW1 from 20K_0402_1% (SD034200280) to 1K_0402_1% (SD034100180) Change the PCW27 from pop to un-pop, and . PCW27.2 net name change from +1.35VSDGPU to Vsense_+1.35VS_VGAP. unpop PCV135 Change the PUV8, PCV9 from pop to un-pop. Add location PRV51 0_0402_5% (SD028000080), and pop. Change the PCW21, PCW22 From 4700P_0402_50V (SE074472K80) to 2200P_0402_50V(SE074222K80). Delete PL1111 (HCB2012KF-121T50_0805)	11/14	A
02	Design Update	solution change	83, 85 90, 91	Change the PQB2,PQM2 from AON7506 (SB000010A00) to EMB12N03V (SB00001HV00) update location PR65 PRA3 to PUG1 PUA1 PLZ1,PLG1,PLZ2,PLZ3,PLZ4 change to common part P/N (SH00001EE00) pop PQZ2, PQZ4 unpop PQZ1, PQZ3	11/16	A
03	Design Update	0 ohm to R-short	83, 85 90, 91	Change PRM10, PRM8, PRV82, PRV85, PRV92, PRV95, PRV79, PRV81, PRV84, PRV89, PRV91, PRV94, PRV54, PRV56, PRV70, PRV145, PRV146, PRZ72, PRZ73, PRZ25, PRZ30, PRZ32, PRZ18, PRZ9, PRZ11, PRZ24, PRZ27,PRV20, PRV34	11/16	A
04	Design Update	For CPU transient	89, 92	change PRZ12 from 1.78K_0402_1%(SD00000WY80) to 1.62K_0402_1%(SD000003380) change PRZ14 from 31.6K_0402_1%(SD034316280) to 28K_0402_1%(SD034280280) change PCZ24 from 470P_0402_50V8J(SE071471J80) to 220P_0402_50V8J(SE082221J80) change PRZ51 from 84.5K_0603_1%(SD014845280) to 100K_0603_1%(SD014100380) PRZ61=110k ohm @H82, PRZ61=102k ohm @H62 PRZ35=25.5k ohm @H82, PRZ35=28k ohm @H62 unpop PCZ101, PCZ103, PCG102 pop PCZ176 un pop PCZ120, PCZ104, PCZ105, PCZ118, PCZ111, PCZ108, PCZ126, PCZ124 for H82 un pop PCZ120, PCZ104, CZ105, PCZ118, PCZ111, PCZ108, PCZ126, PCZ124, PCZ123, PCZ127, PCZ107, PCZ113, PCZ116, PCZ114 for H62	11/19	A
05	Design Update	solution change	84	Change the PL501 1.5uH to common part Change the PCZ47, PCZ48, PCZ65, PCV36, PCV249 from 33U_25V_NC_6.3X4.5 (SF000007200) to 33U_25V_M (SF000007700) Change the PRZ43 from 12.1K_0402_1% (SD034121280) to 12K_0402_1% (SD034120280)	12/3	A
06	Design Update	solution change	87	unpop PC1811 0.47U_0402_6.3V6K (SE124474K80)	12/12	B
07	Design Update	solution change	83, 97	pop PCV149~PCV158, PCV162~PCV165, PCV258 (1U_0201_6.3V6M) reserve PDB2 for dead battery	12/18	B
08	Design Update	solution change	87, 93, 94	Change PR1010, PRW9, PR1801, PR2501 from 0ohm to r-short	12/18	B
09	Design Update	For ESD request	82	Pop PC205 0.1U_0603_25V7K (SE042104K80) HS 陶瓷 鋁 皮 膜 電 容 ,ESD 能 量 透 過 率 低 coupling 鍍 板 造 成 的	1/15	B
10	Design Update	For EMI request	93, 96	Pop PCW1, PCV48 2200P_0402_50V7K (SE074222K80) for EMI request Pop PCW2, PCV47 0.1U_0402_25V6 (SE000006880) for EMI request	1/15	B
11	Design Update	Design change	90, 87	delete boost circuit and PCZ47	5/7	FH58F EVT
12	Design Update	Design change	90, 87	delete PC1112	5/7	FH58F EVT
13	Design Update	Design change	88, 93	change PCB15 from S CER CAP 1U 6.3V K X5R 0402(SE000000K80) to 1U 16V K X5R 0402(SE000000U00) change PCB16 from S CER CAP 1U 6.3V K X5R 0402(SE000000K80) to S CER CAP 2.2U 16V K X5R 0402(SE000013780) Add PLV2, PLV3 second source S COIL .22UH TMP C1004H-R22MG-R5505-D 50A(SH00001XH00)	6/25	INV2
14	Design Update	change CH_OC to 75A	95	change PRV71 from S RES 1/16W 133K +-1% 0402(SD034133380) to S RES 1/16W 113K +-1% 0402(SD034113380)	6/25	FH58F PVT

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1	52	CNVi	1205B	CNVi-Intel review (FH5VF)	Add RM67 / RM68 0-ohm Add PU RM70 / PD RM69 (Reserve)
2	52	UART_BT	1205B	UART_BT review	RM66 Change to @ for Vender review
3	81-111	PWR SCH	1206A	POWER update	Combined Power SCH (1204)
4	40	HDMI	1206B	HDMI EMI solution	Remove RY52/RY53/CY27 , LS15 change to pop (EMI@) .
5	17/69	JSSD3	1206B	JSSD3 SATA/PCIE detect	SATA6P change to 6P4 & RH303 PU
6	64	EMR	1206B	EMR Power source	RH285/RH286/RH292 power source change to +3VALW
7	63	Touch Pad	1206B	ESD	Add CK203(100p) for ESD
8	27	VGA	1206C	CLKREQ	RV83 change to pop(VGA@) / CV226 change to unpop (@)
9	19	PROJECT ID	1206C	PROJECT ID	defined as Project - 50 ( ID1:H / ID0:L )
10	38	Panel OD	1206C	Panel OD function	RX11 change to unpop & BIOS needs to detect panel to select H or L .
11	16/58	BT_ON	1206C	BT_ON change to PCH	RH304 pop (PCH) & RB85 unpop (EC)
12	73	IO_B conn.	1209A	IO_B conn.	IO_B change pin define
13	15/68/69	M.2 SSD	1209B	Fixed naming	> SSD1 - GPP_B9/CLKREQ4# (PCIE only) (2018 @SSD2) > SSD2 - GPP_B8/CLKREQ3# (PCIE/SATA) (2018 @SSD1) > SSD3 - GPP_B10/CLKREQ5# (PCIE/SATA) (2019 NEW)
14	52	CNVi	1209B	CNVi-Intel review (FH5VF)	RM70 change power source to +3VS_WLAN
15	81-111	PWR SCH	1209C	POWER update	Combined Power SCH (1209)
16	81-111	PWR SCH	1210A	POWER update	Combined Power SCH (1209B)
17	77	H6	1210B	For Layout	H6 change to GND A for Layout .
18	69	SSD3	1210B	BOM Config	ADD "SSD3@" for BOM
19	58	Board ID	1210B	Board ID config	ADD DVT@ & DVTRGB@ for DVT BOM
20	52	CNVi	1210C	CNVi-Intel review (FH51M)	> RM69 change to 71.5k & CNVi@ > RM70 set CNVi@ > RH22 change to 20K > RM36/RM37/RM67/RM68 change to 22 ohm
20	63	ESD	1211B		> Pop CK203 680p & ESD@ > CB12/CB13 change to 33p for ESD & ESD@

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